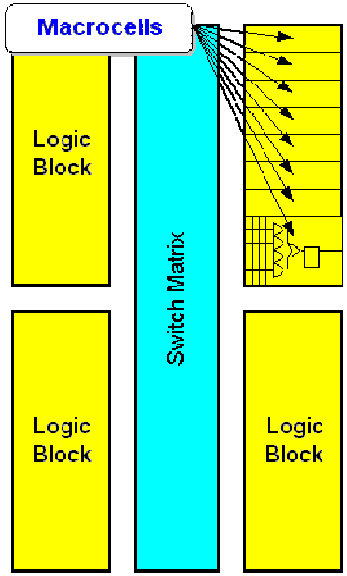
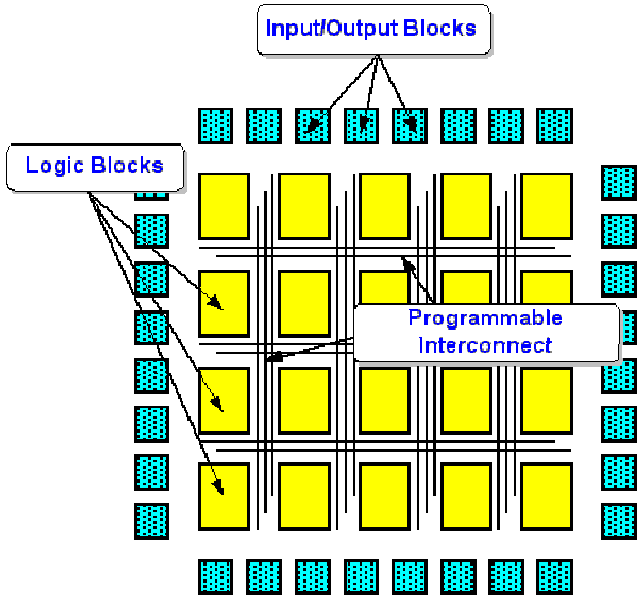
Hardware platform

Agenda

- **Architecture of FPGAs**
- **Xilinx Artix-7 family**
- **Digilent Nexys A7 platform (form. Nexys4 DDR)**

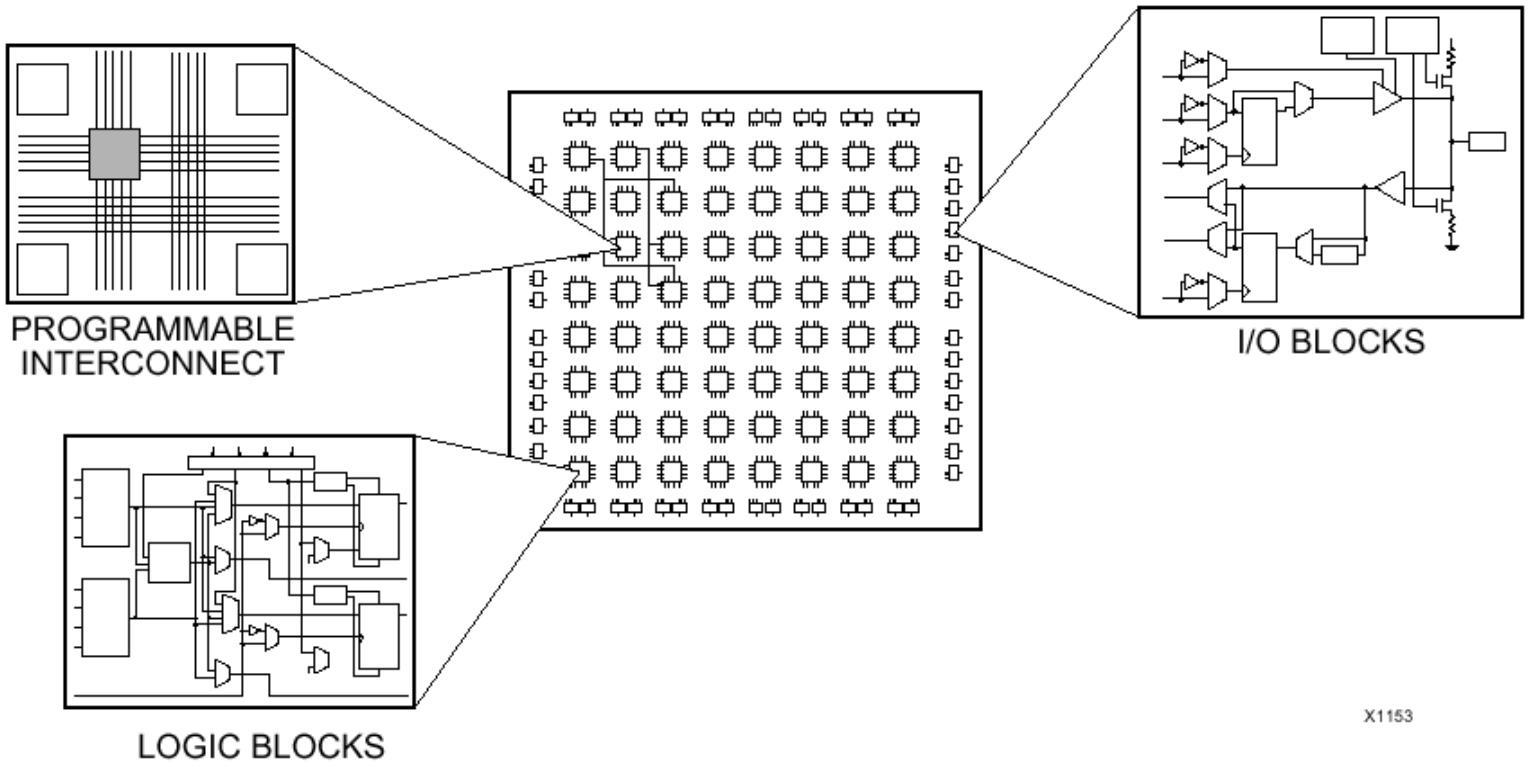
Architecture of FPGAs
CPLD vs FPGA





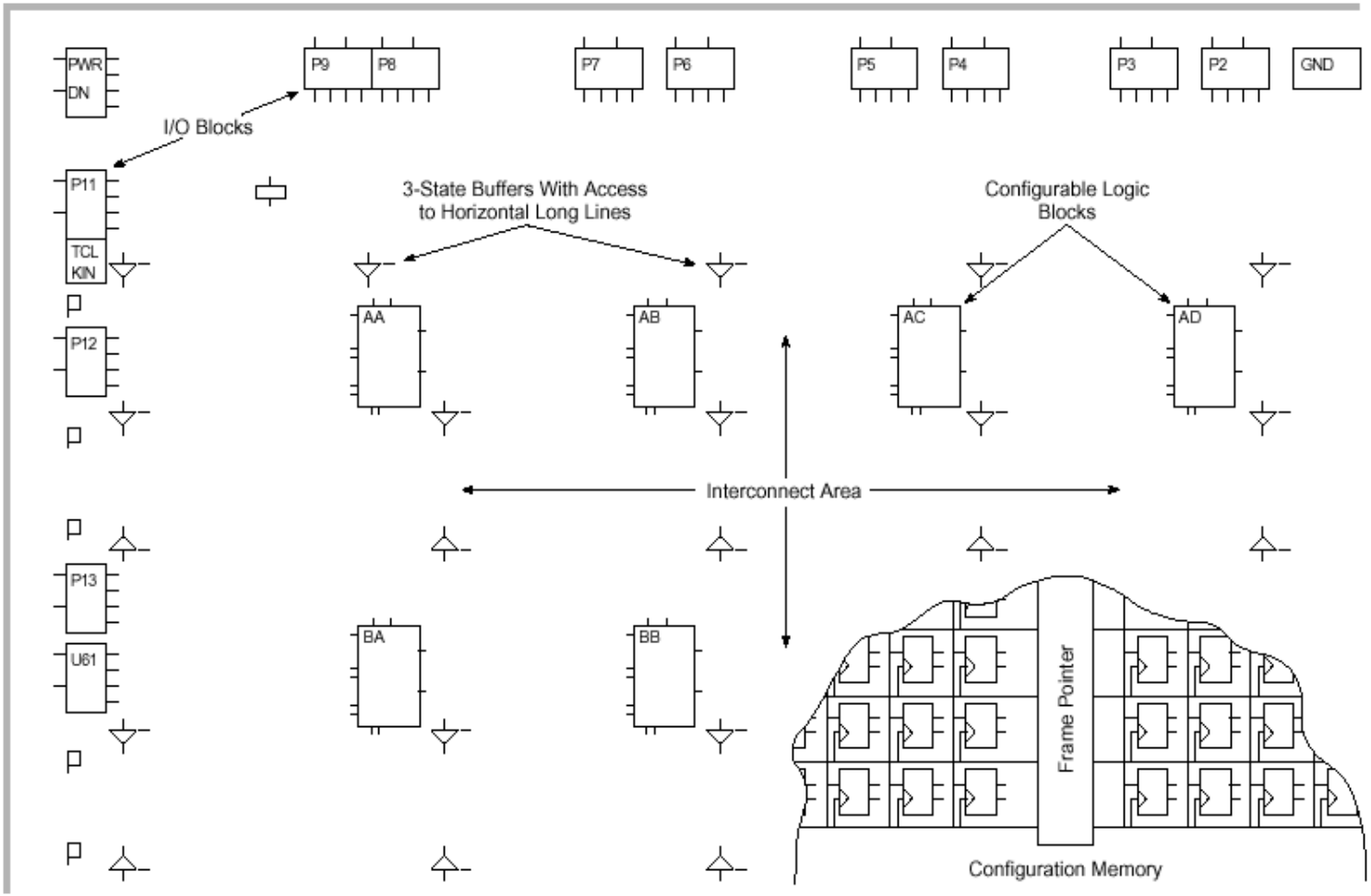
PAL type more combinational logic	ARCHITECTURE	Gate Array type more flip-flops
small / mid multiple 22V10 structure	DENSITY	mid / large / very large up to ~10 million gates
up to ~300 MHz predictable delays	SPEED	up to ~1000 MHz dependent delays
fixed connection matrix	CONNECTIONS	segmented programmable connections

User resources

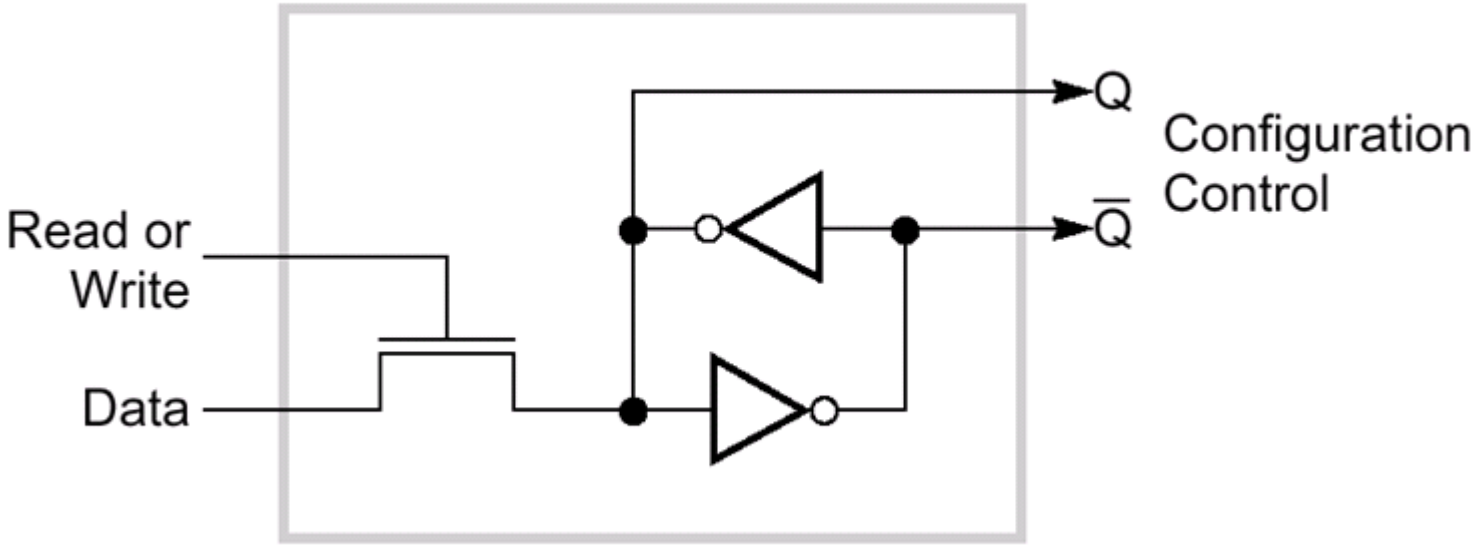


- **Input Output Blocks**
- **Configurable Logic Blocks** (and other specialized)
- **Programmable Interconnect Resources**

User resources and configuration memory

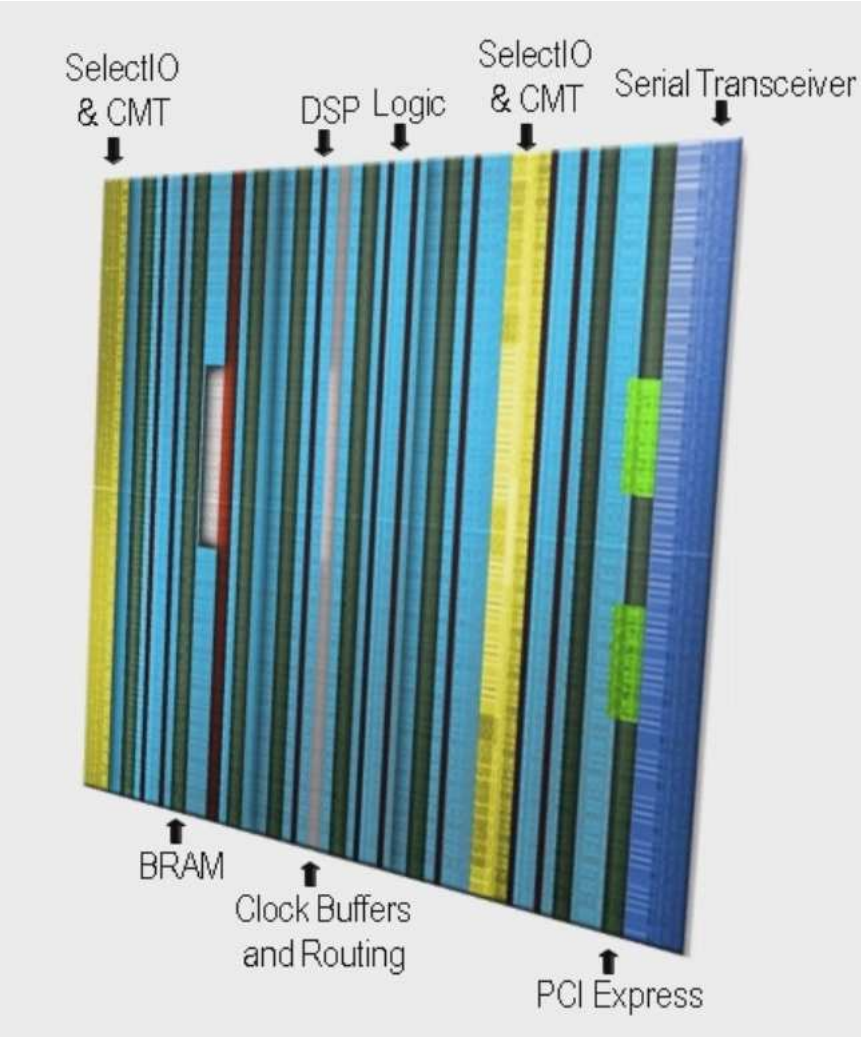


Configuration memory



- written during configuration and read during verification
- during normal operation transistor switched off
- one data bit controls one configuration point
- non-sensitive to large alfa ray doses

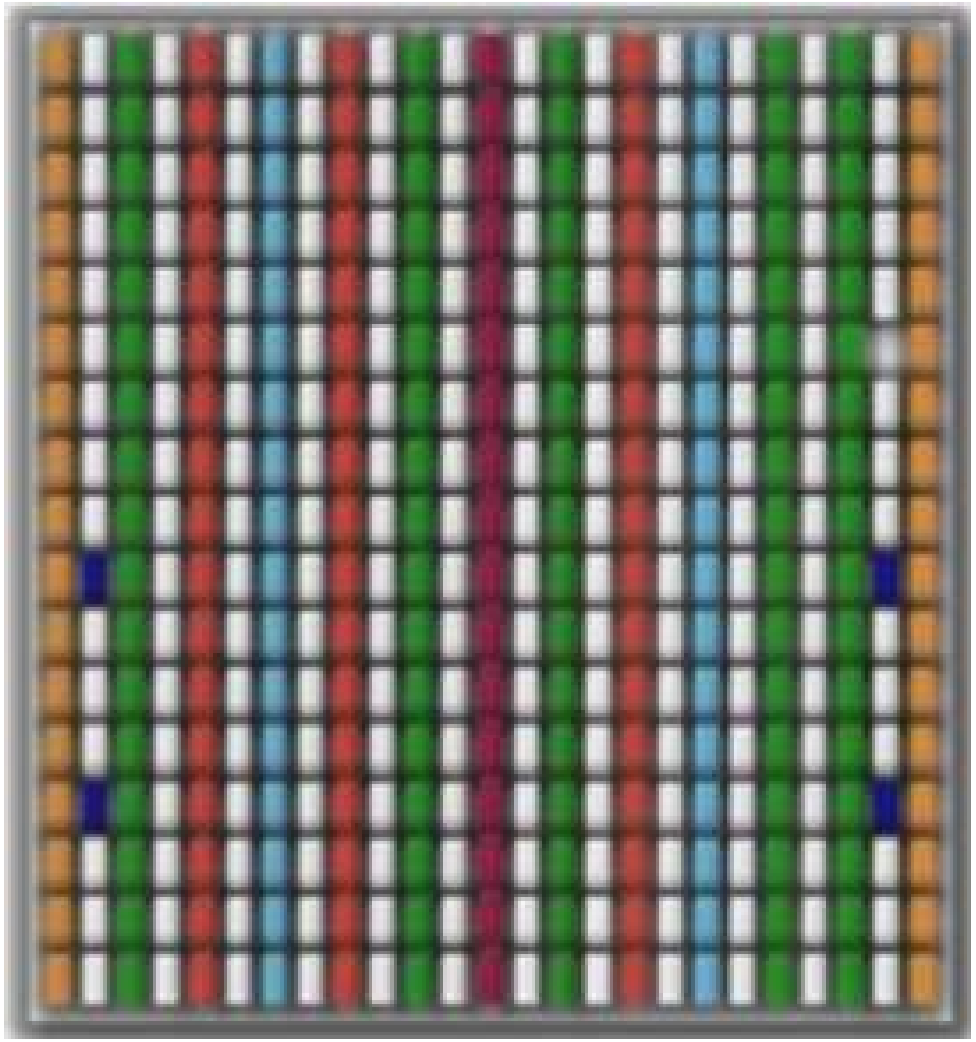
Xilinx Artix-7
Basic features



- 28 nm technology
- coarse-grain structure
- 13k – 215k logic cells
- 16k – 270k flip-flops
- 1412 MHz max toggle frequency
- clocks – CMTs: 3…10
- Select RAM+ user memory
  - distributed: up to 2888 Kb
  - block: up to 13140 Kb
  - external
- 25b × 18b DSP48 MAC: 40…740
- PCIe ..×4 ..Gen2, GTP: 2…16, XADC
- User I/Os
  - pins: 150…500
  - banks: 3…10
- SRAM configuration memory
- JTAG port (test+configuration)
- power supply :

V_{CCINT} : 0.9…1.0 V V_{CCBRAM} : 0.95…1.0 V
V_{CCAUX} : 1.8 V V_{CCO} : 1.2…3.3V
$V_{MGTAVCC}$: 1.0 V V_{CCADC} : 1.8 V

Xilinx Artix-7
Structure



High Performance Serial I/O Connectivity MGT

High Performance Parallel I/O Connectivity SelectIO

Logic fabric LUT-6 CLB

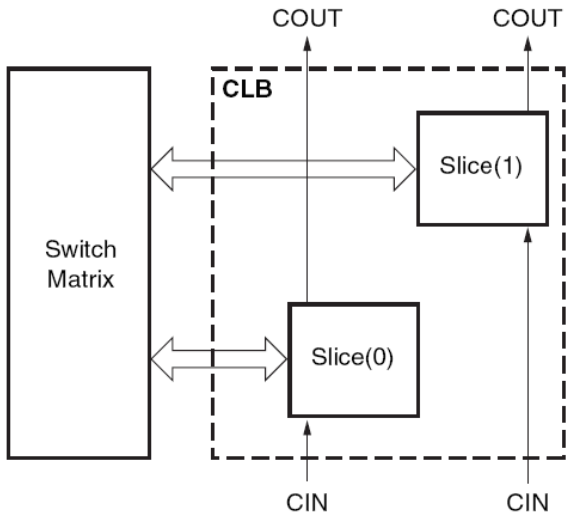
On-Chip Memory 36/18Kb BlockRAM

DSP Engines LUT-6 CLB

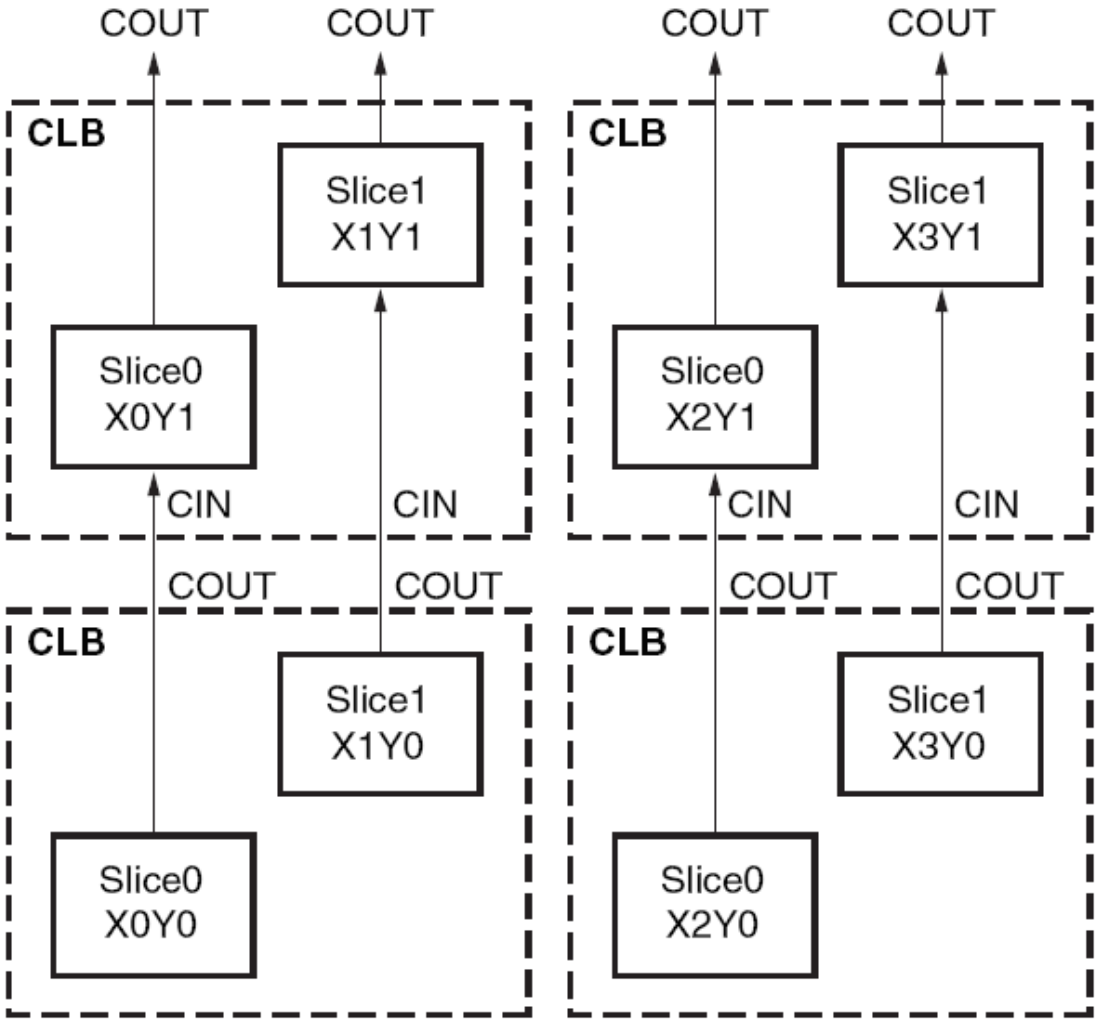
Precise Low Jitter Clocking MMCM

Enhanced Connectivity PCIe

Xilinx Artix-7
Configurable Logic Block



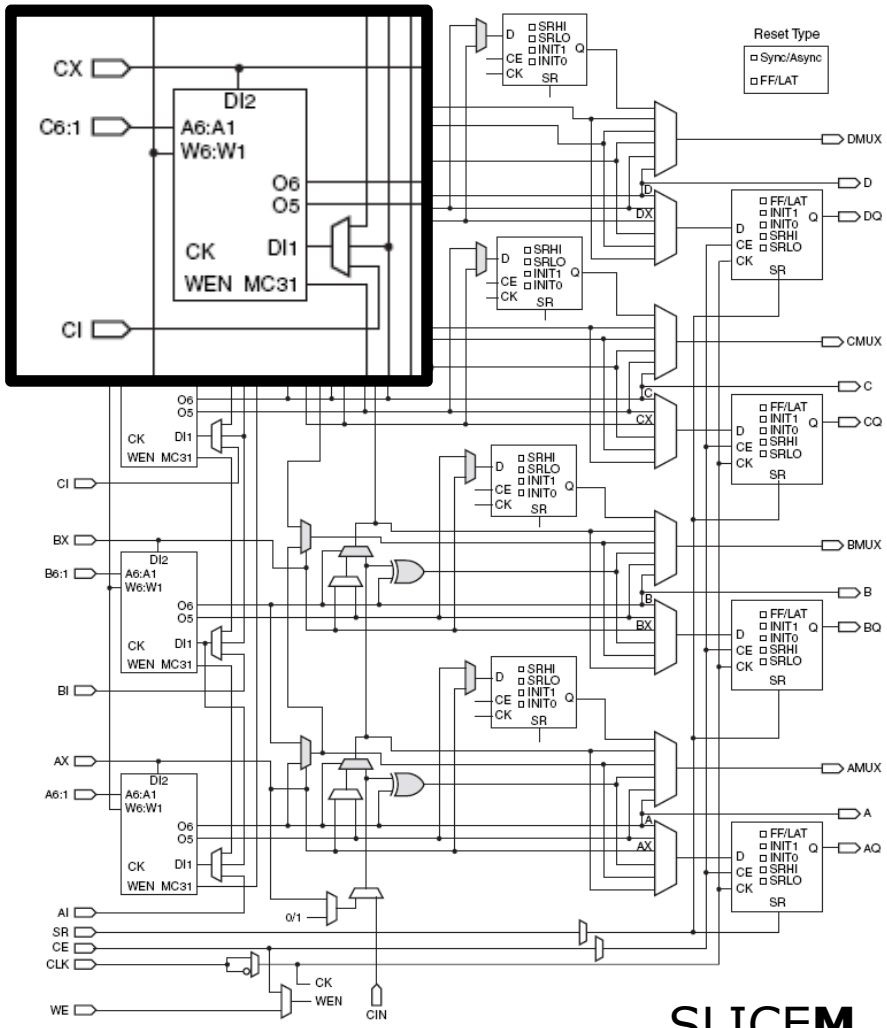
CLB = 2 x LS = 8 x LC



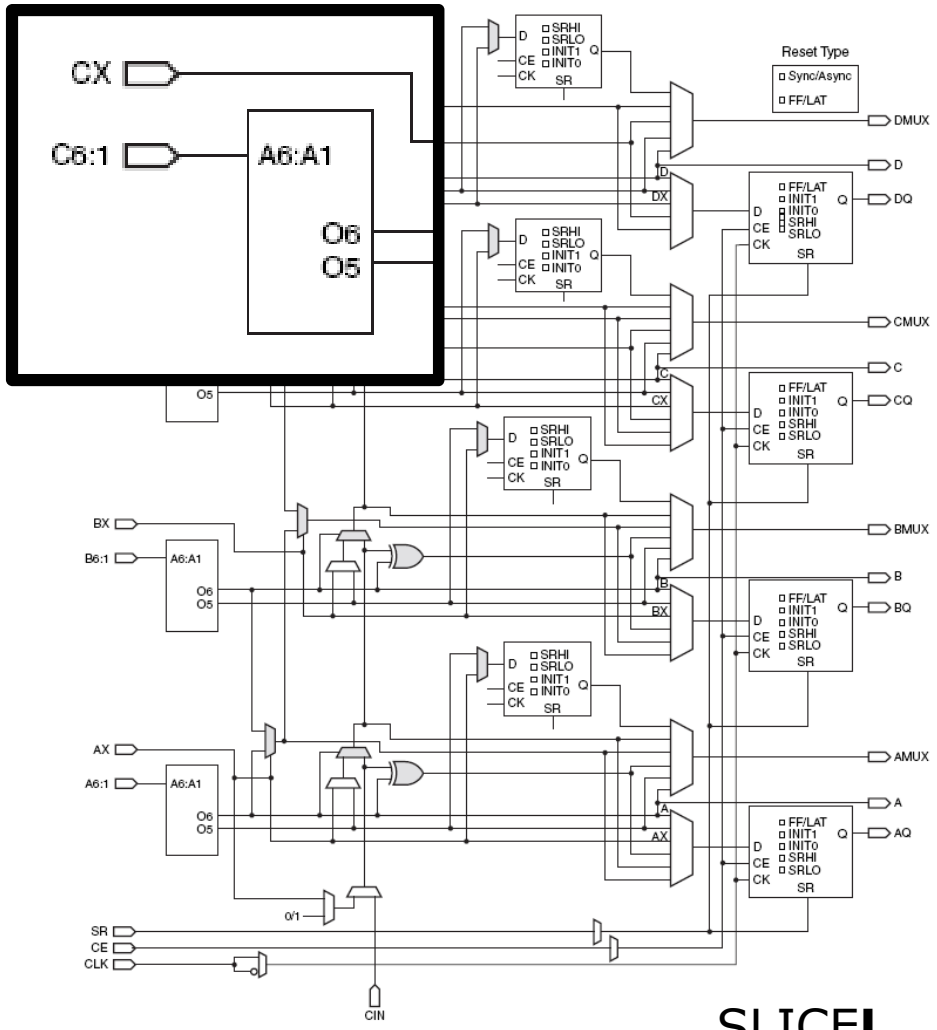
Logic Cell:

- 2 flip-flops / 1 latch
- Clock Enable ☝
- AP / AC / SS / SR
- one 6-input or 2 5-input LUTs (Look-Up-Tables)
- carry logic

Xilinx Artix-7
Logic Slice



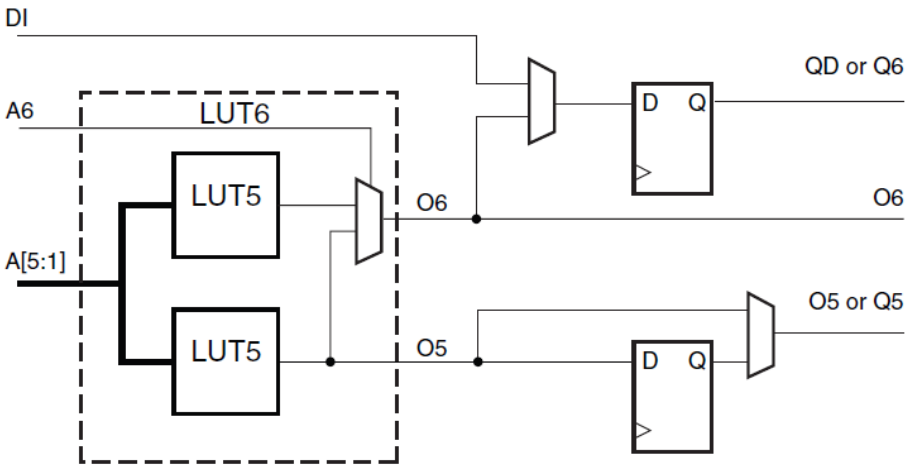
SLICE**M**



SLICE**L**

Logic Cell

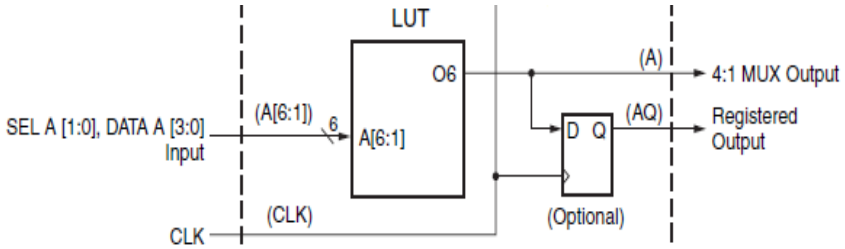
Feature	SLICEL	SLICEM
6-Input LUTs	√	√
8 Flip-flops	√	√
Wide Multiplexers	√	√
Carry Logic	√	√
Distributed RAM		√
Shift Registers		√



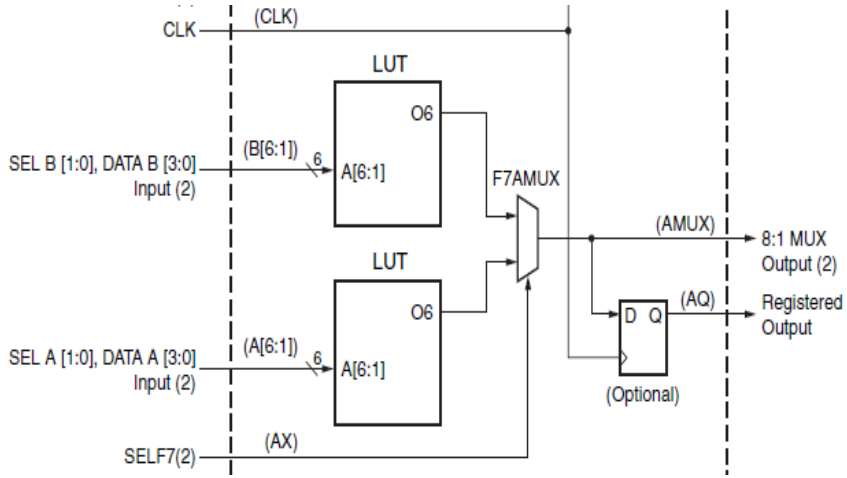
LUT6:

- **6-input function generator**
- **SinglePort / DualPort RAM**
- **32-stage shift register**

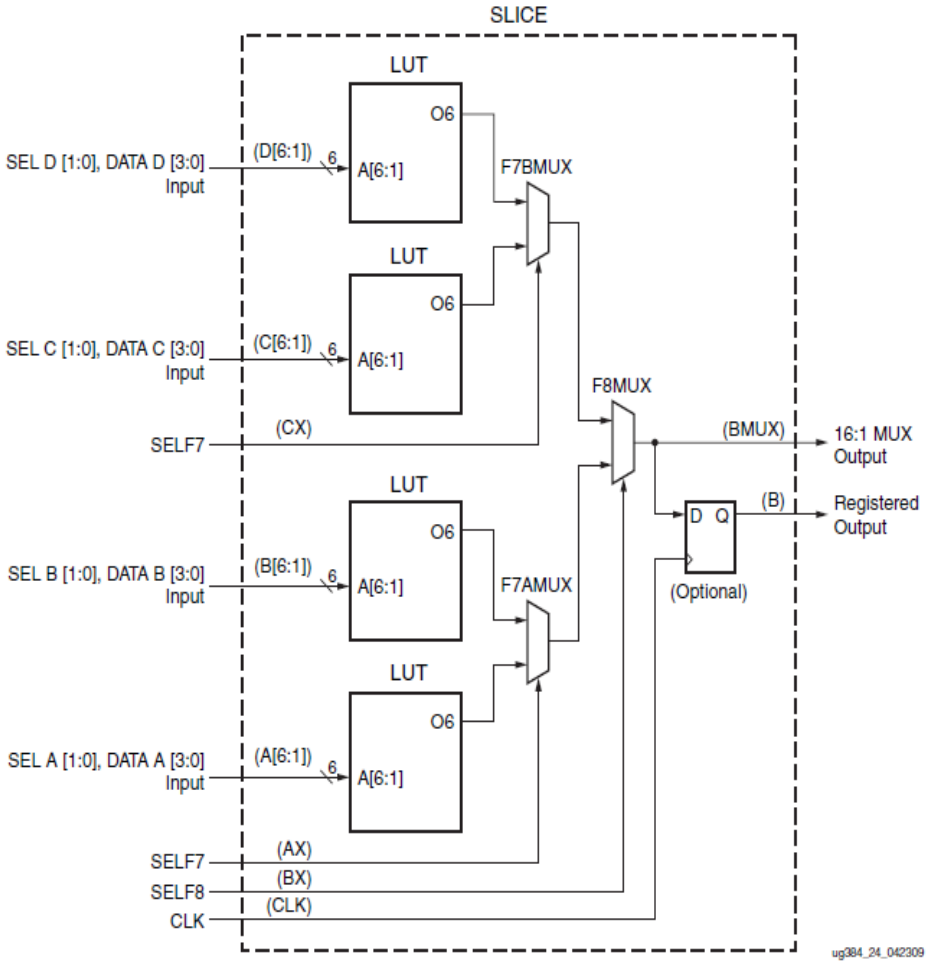
Configurable Logic Block: LUTs & multiplexers



Mux 2:1 / Fun 6-in

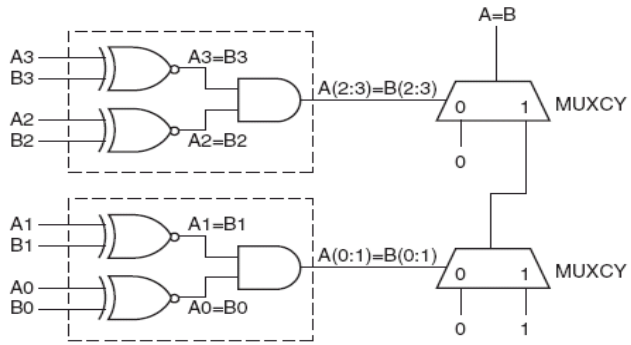


Mux 4:1 / Fun 7-in (up to 13-in)

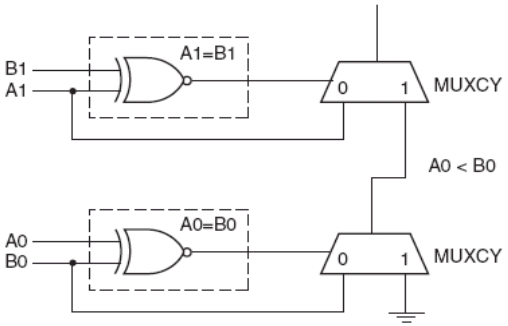


Mux 8:1 / Fun 8-in (up to 27-in)

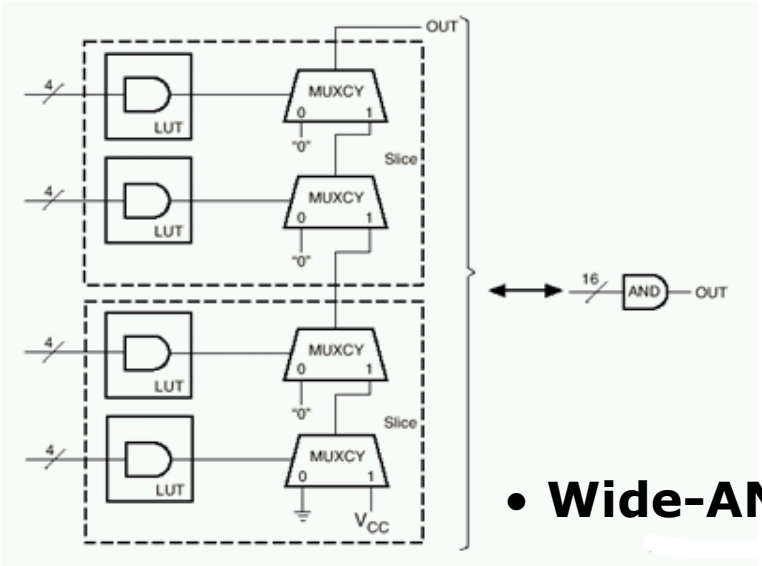
Configurable Logic Block: Carry & Arithmetic



- **Equality Comparator**

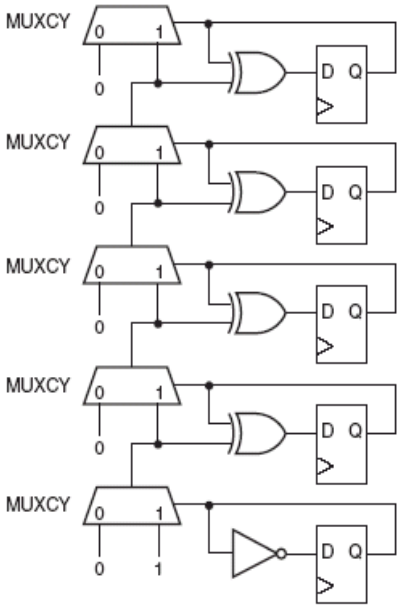


- **Magnitude Comparator**

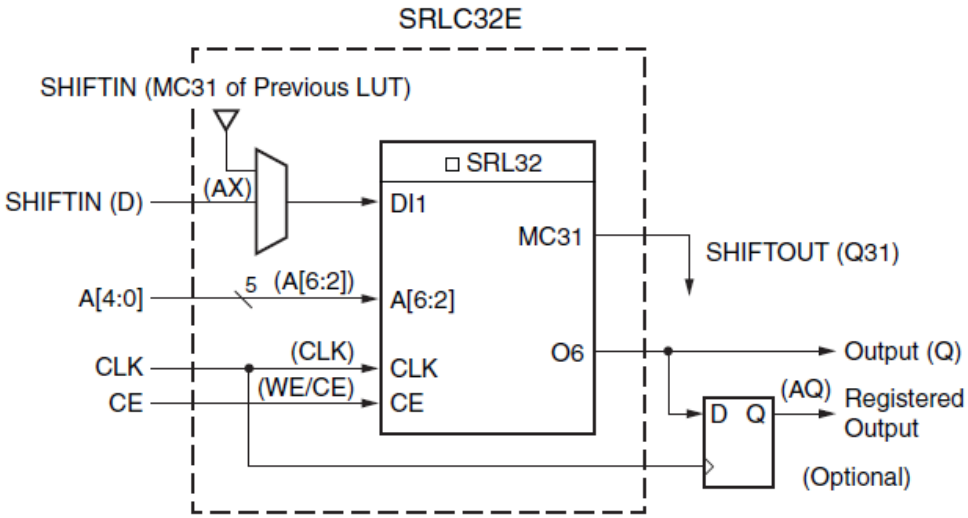


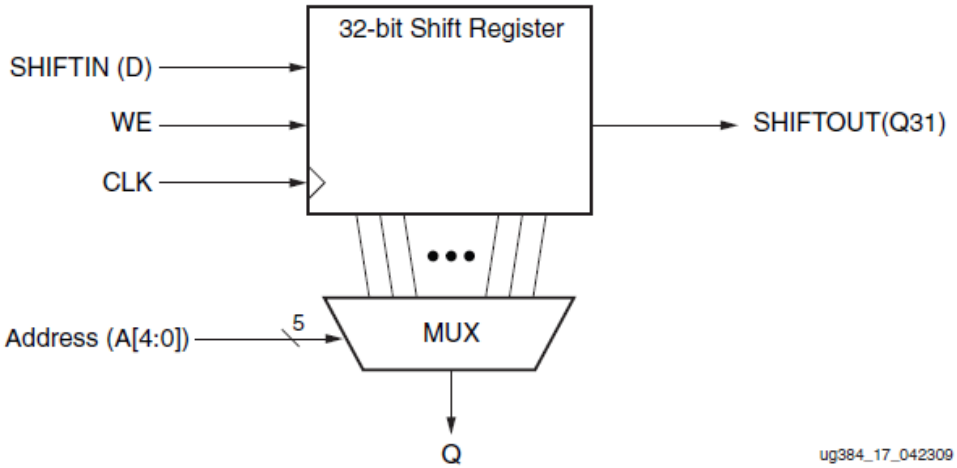
- **Wide-AND**

- **Counter**



LUT: SRL Shift Register





Applications:

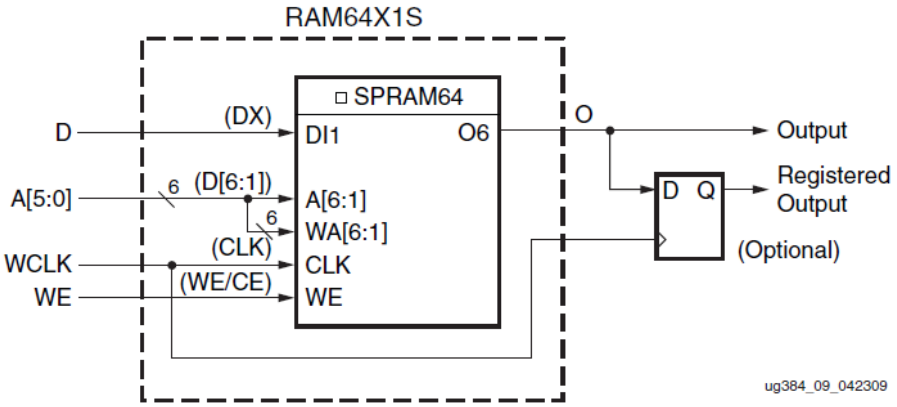
- long delay lines
- long counter (also LFSR)
- synchronous FIFO
- pseudo-random generators

Configurations:

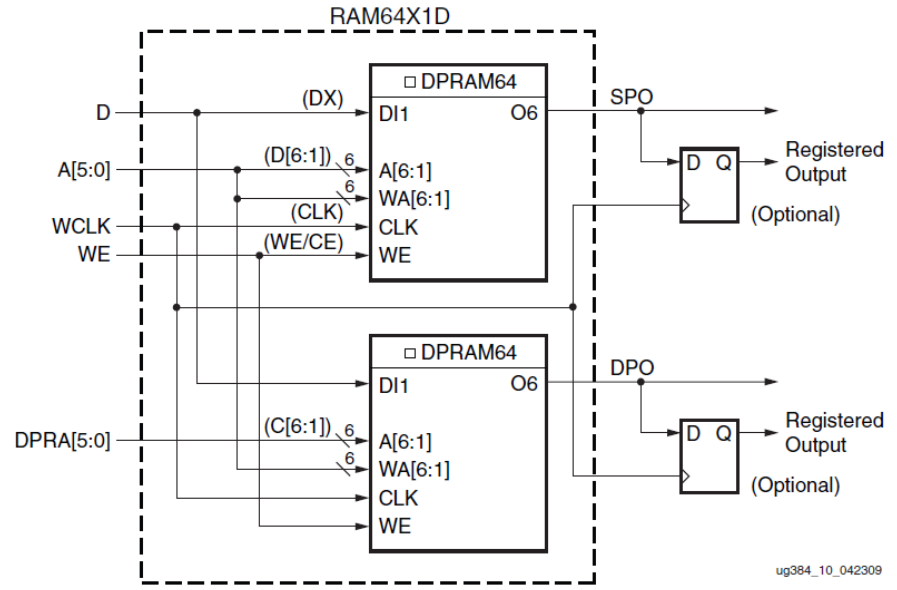
- single 32-bit
- double 16-bit
- cascaded: 64, 96, 128-bit
- longer – with general interconnect resources

Xilinx Artix-7
LUT: Distributed RAM

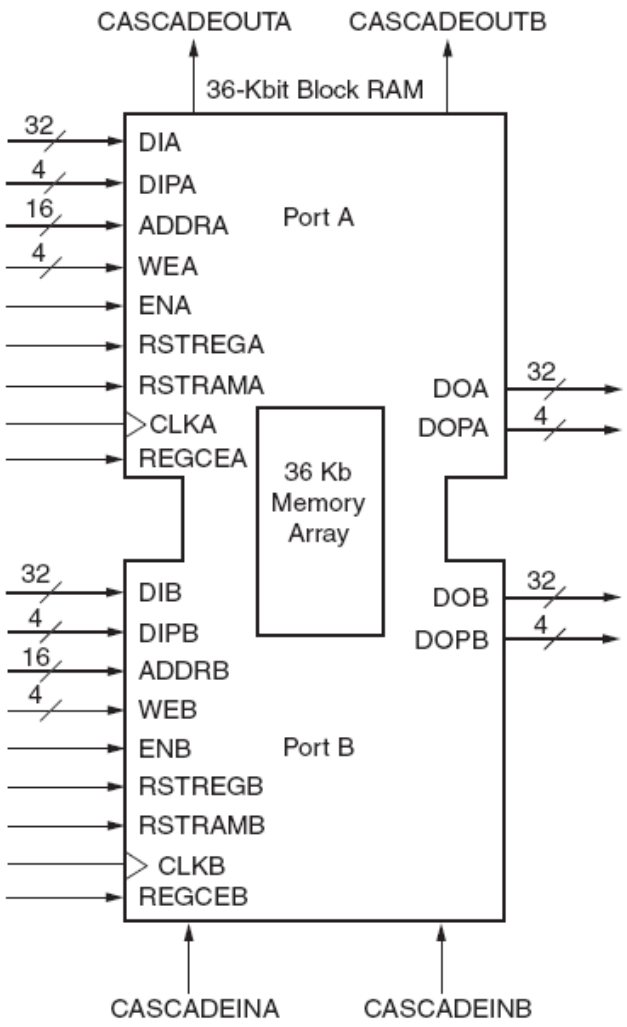
ROM	Number of LUTs
64 x 1	1
128 x 1	2
256 x 1	4

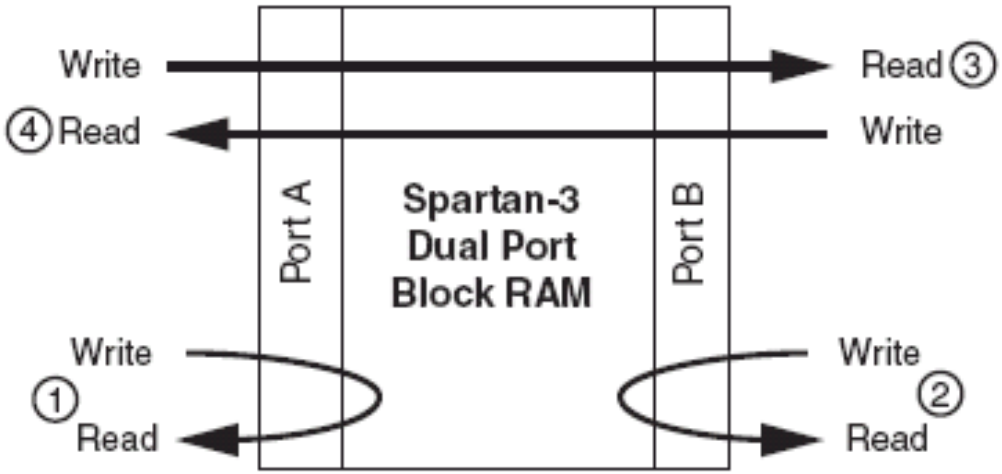


RAM	Description	Primitive	Number of LUTs
32 x 1S	Single port	RAM32X1S	1
32 x 1D	Dual port	RAM32X1D	2
32 x 2Q	Quad port	RAM32M	4
32 x 6SDP	Simple dual port	RAM32M	4
64 x 1S	Single port	RAM64X1S	1
64 x 1D	Dual port	RAM64X1D	2
64 x 1Q	Quad port	RAM64M	4
64 x 3SDP	Simple dual port	RAM64M	4
128 x 1S	Single port	RAM128X1S	2
128 x 1D	Dual port	RAM128X1D	4
256 x 1S	Single port	RAM256X1S	4



Xilinx Artix-7
Block RAM

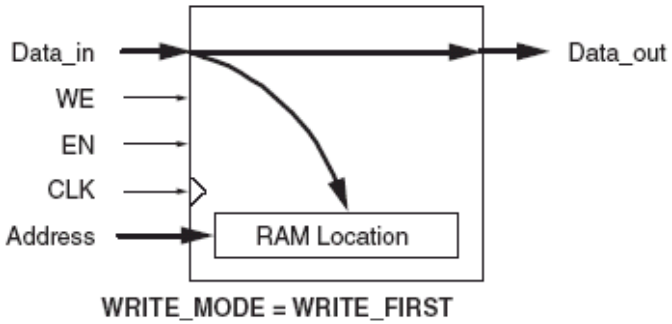




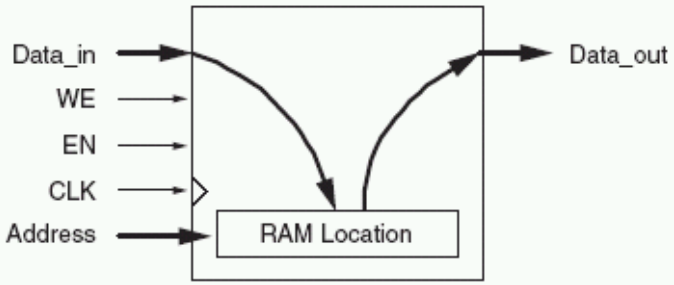
- **single 36Kb block or double 18Kb blocks**
- **Single-Port, Dual-Port (Simple/True Mode)**
- **cascadable**
- **ECC**

64K × 1 (cascaded)
32K × 1
16K × 2
8K × 4
4K × 9 (parity)
2K × 18 (parity)
1K × 36 (parity)
512 × 72 (parity, simple)

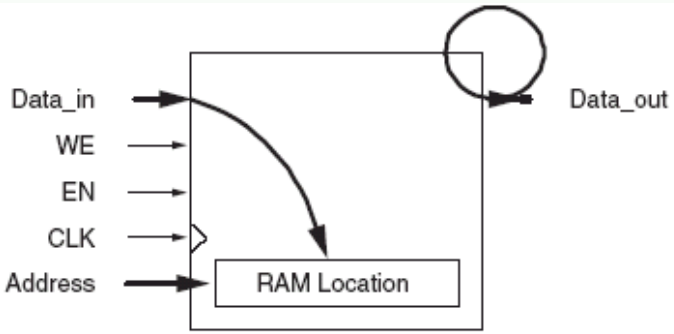
Block RAM



WRITE_MODE = WRITE_FIRST



WRITE_MODE = READ_FIRST

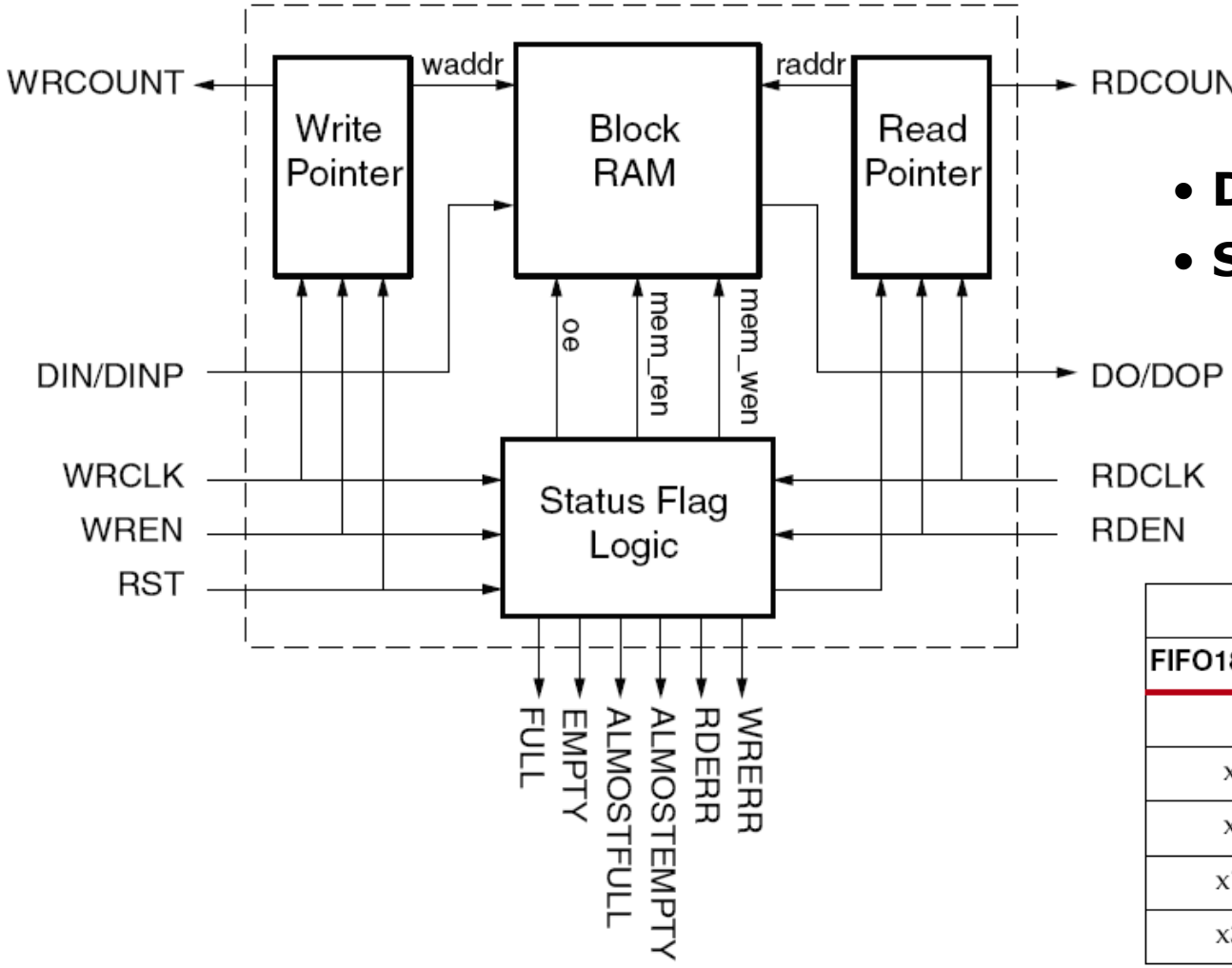


WRITE_MODE = NO_CHANGE

Applications:

- large memories (combined)
- Read Only Memories
- FIFO registers
- μP code memory
- circular buffers
- delay lines
- complex FSMs
- complex combinational functions
- fast, long counters
- Context Addressable Memories
- 4-port memories
- tabelarized math functions (DDS)

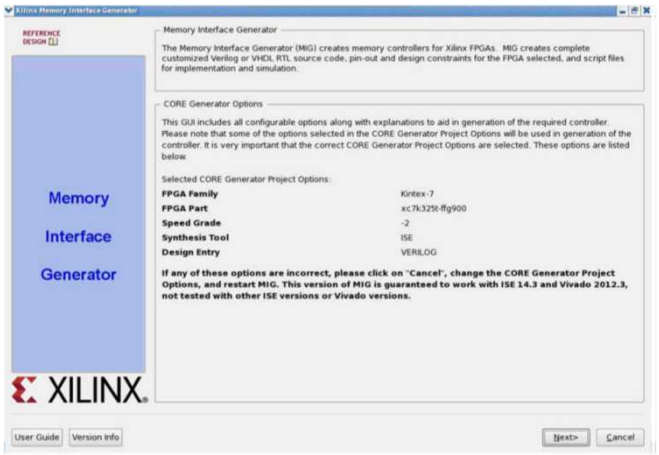
Block RAM FIFO



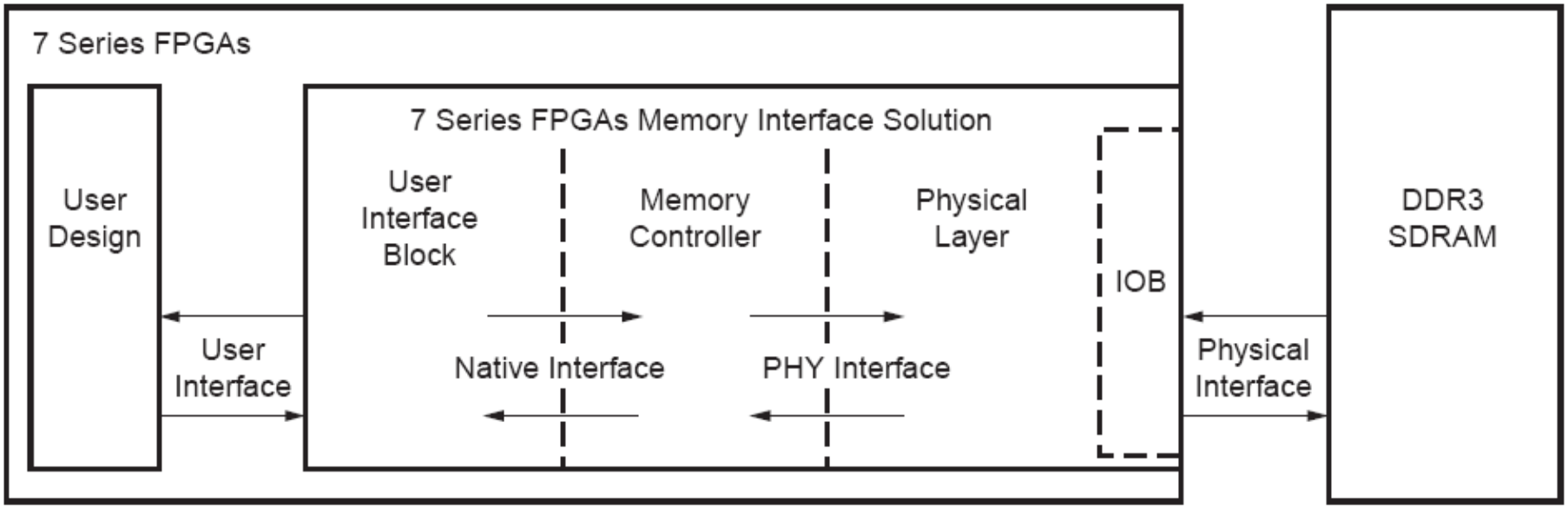
- **Dual-Clock FIFO**
- **Synchronous FIFO**

Data Width		Block RAM
FIFO18 Mode	FIFO36 Mode	
	x4	8192
x4	x9	4096
x9	x18	2048
x18	x36	1024
x36	x72	512

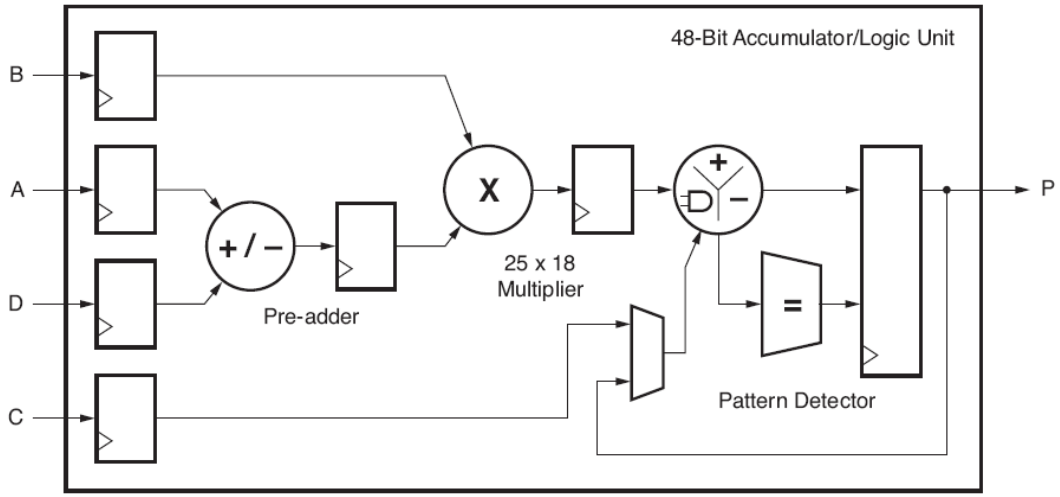
Xilinx Artix-7
Memory Interface Solution



- **DDR3 i DDR2**
- **QDDRII+ SRAM**
- **RLDRAM II / III**
- **internal interface up to 72-bit**
- **1…4Gb**
- **8/16-bit external ports**
- **clock up to >1 GHz**



Xilinx Artix-7
DSP48E1 block

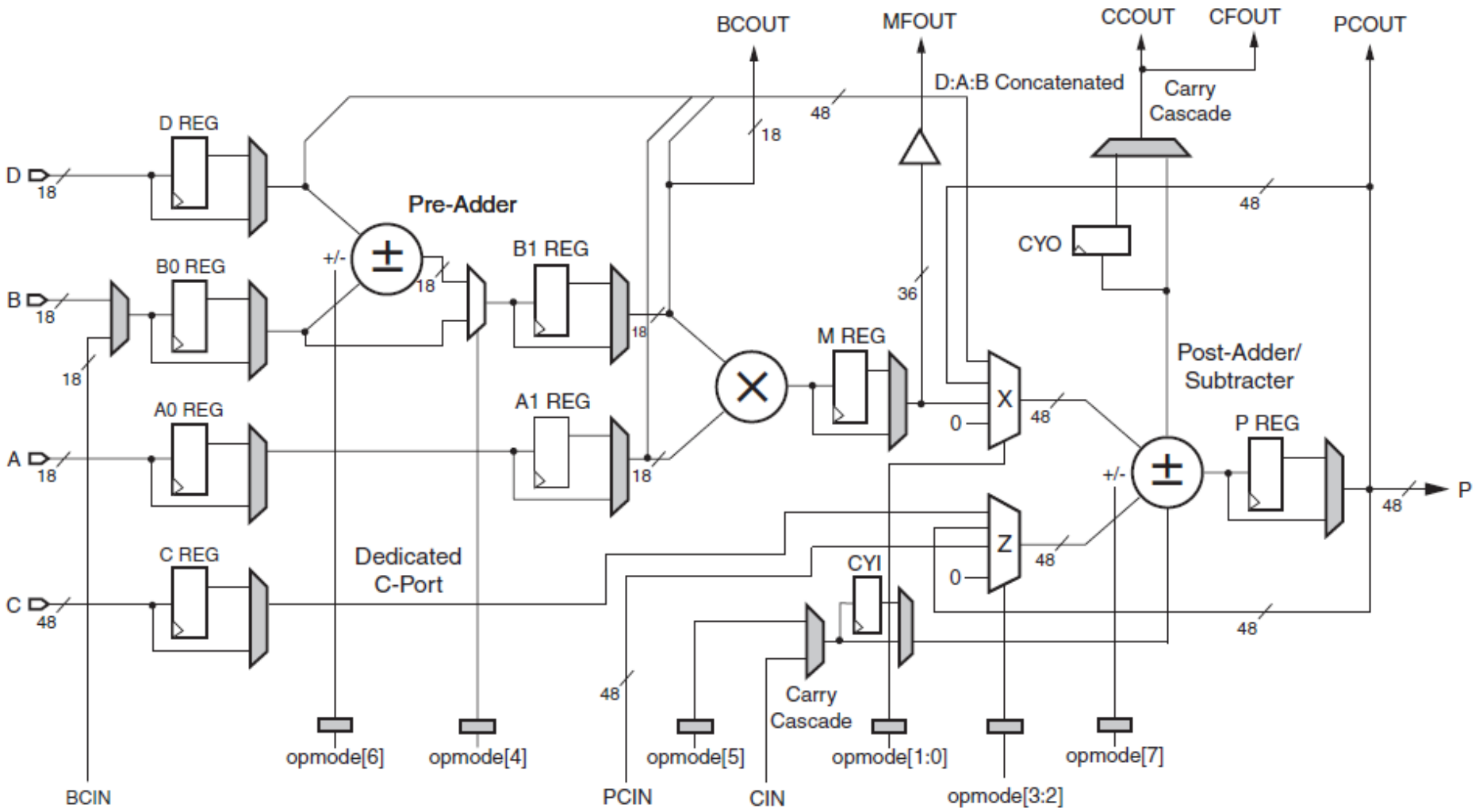


- 25b × 18b factors
- 48b accumulator
- preadder
- logic function generator
- 2’s complement
- optional regisetrs
- combining into larger
- splitting onto smaller
- pattern detector

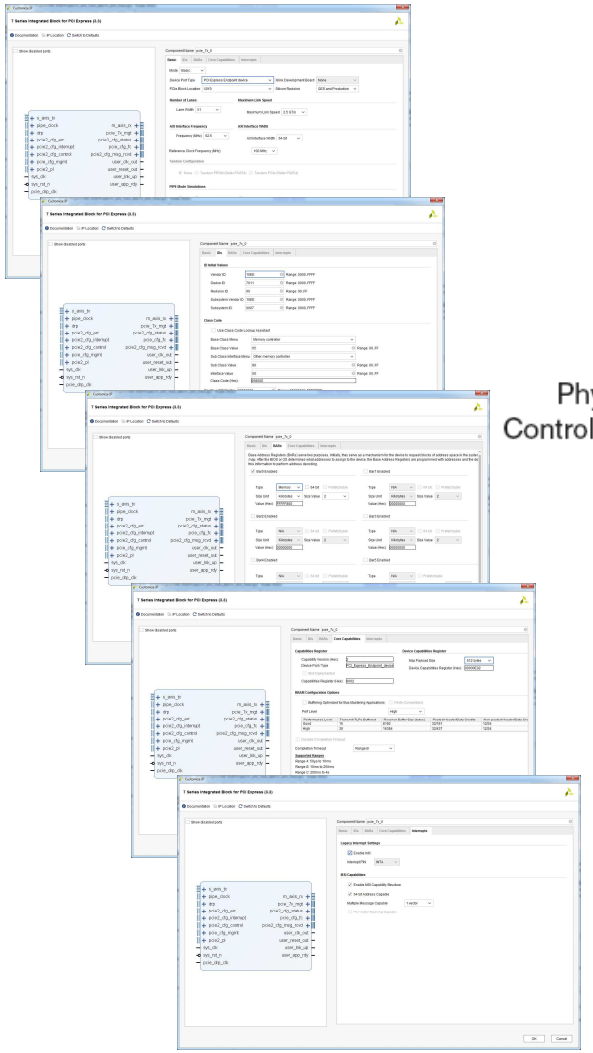
Zastosowania:

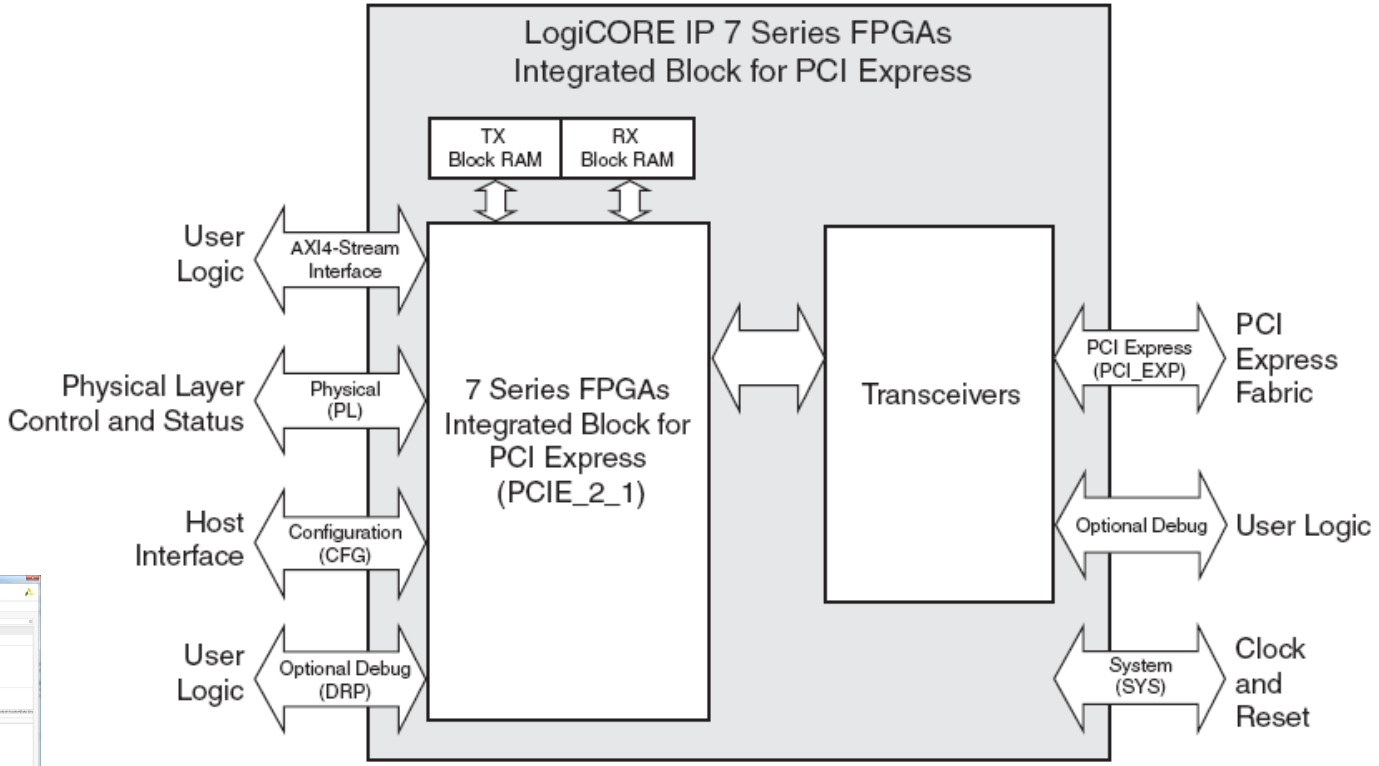
- multiplication
- shifting
- logic functions
- module calculation
- 2’s complement generation
- complex numbers multiplication
- matrix multiplication (with time sharing)
- floating numbers multiplication

Xilinx Artix-7
DSP48E1 block



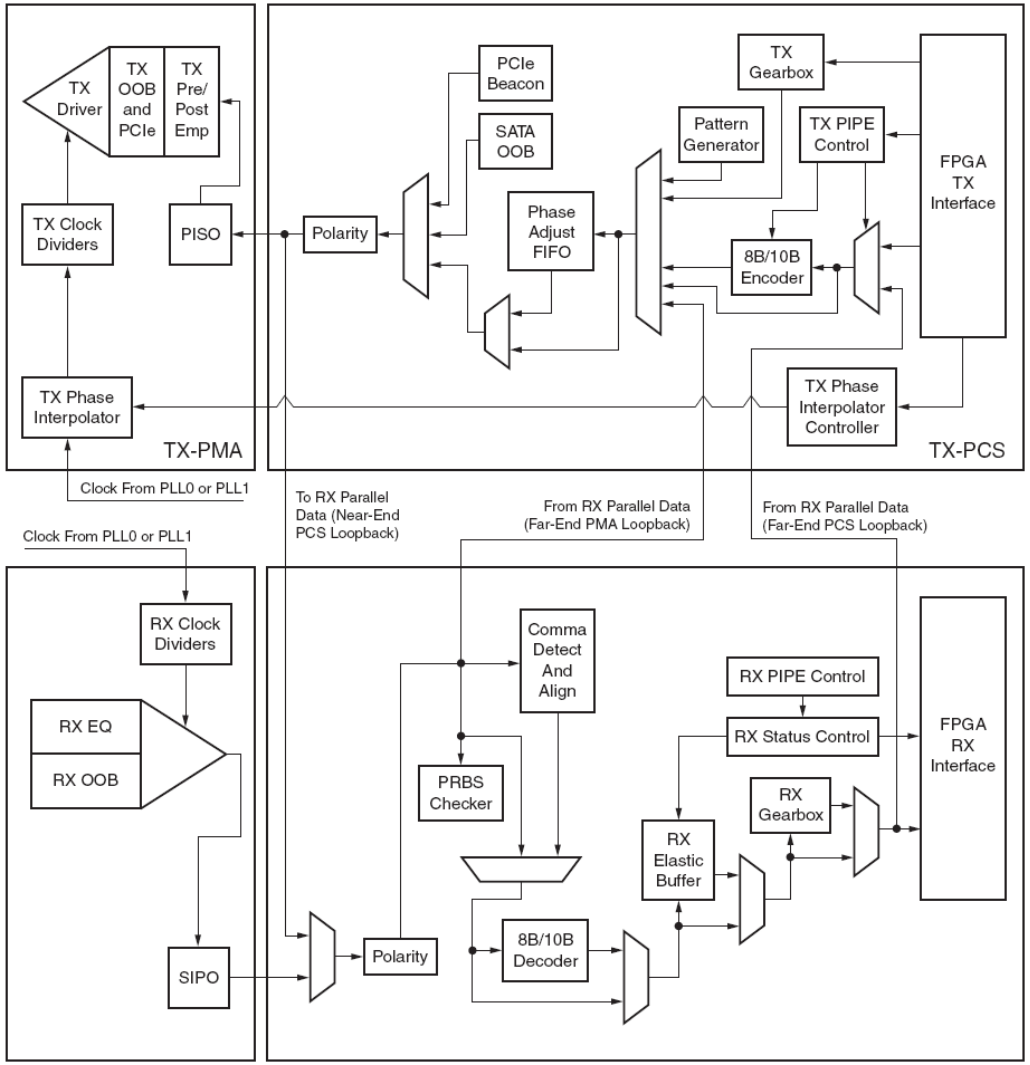
Xilinx Artix-7
PCIe Integrated Endpoint Block



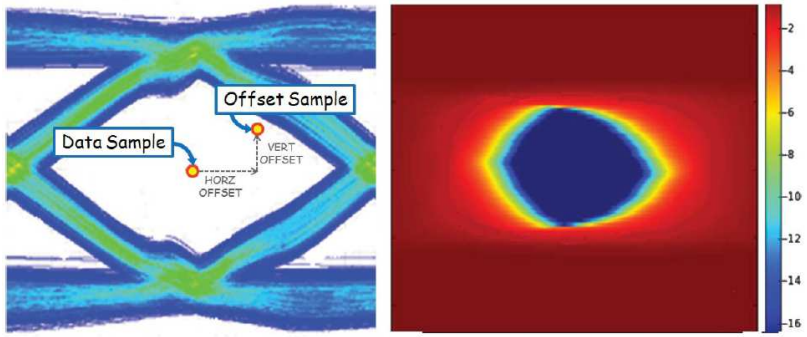


- **1 controller**
- **64/128-bit data bus**
- **×1…×4 lanes**
- **Gen1/Gen2 (2.5/5.0 Gbps)**

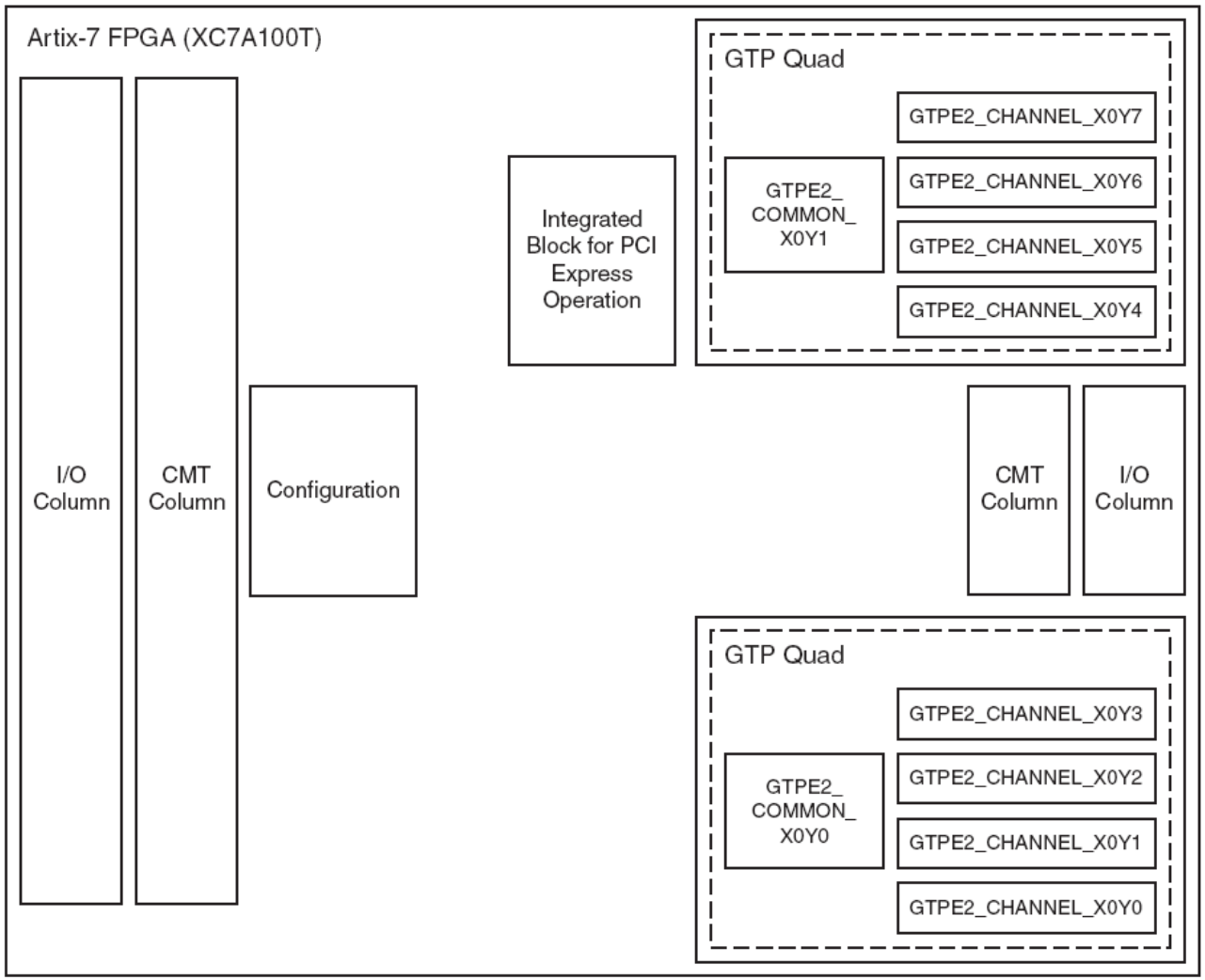
Xilinx Artix-7
GTP Transceivers

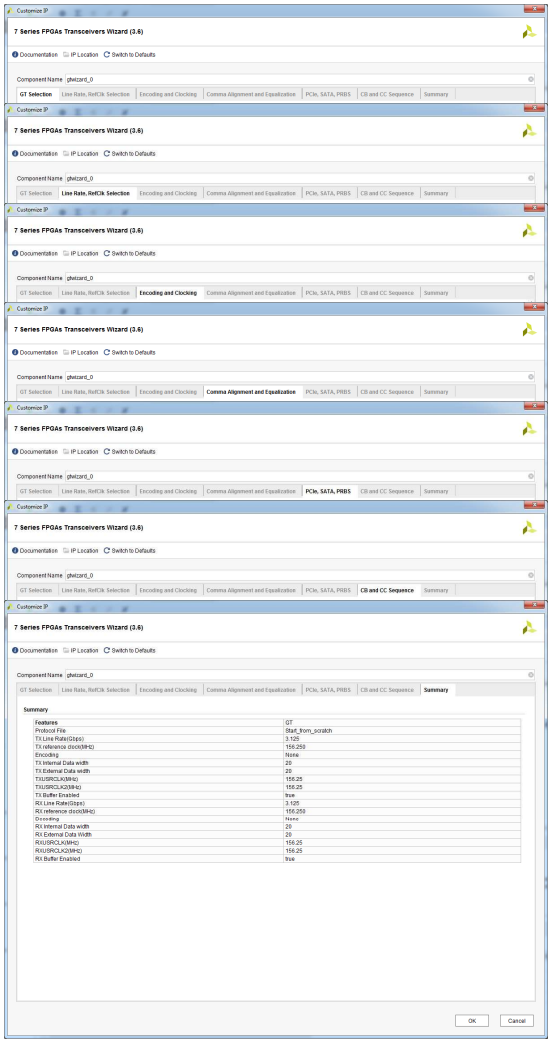


- up to 16 transceivers
- lane rate range:
  0.5…6.6 Gbps
- 8b/10b, gearbox
- suport:
  - PCIe
  - SATA
  - 10GbE XAUI
  - SDI
  - …
- PRBS, h&v eye-scan

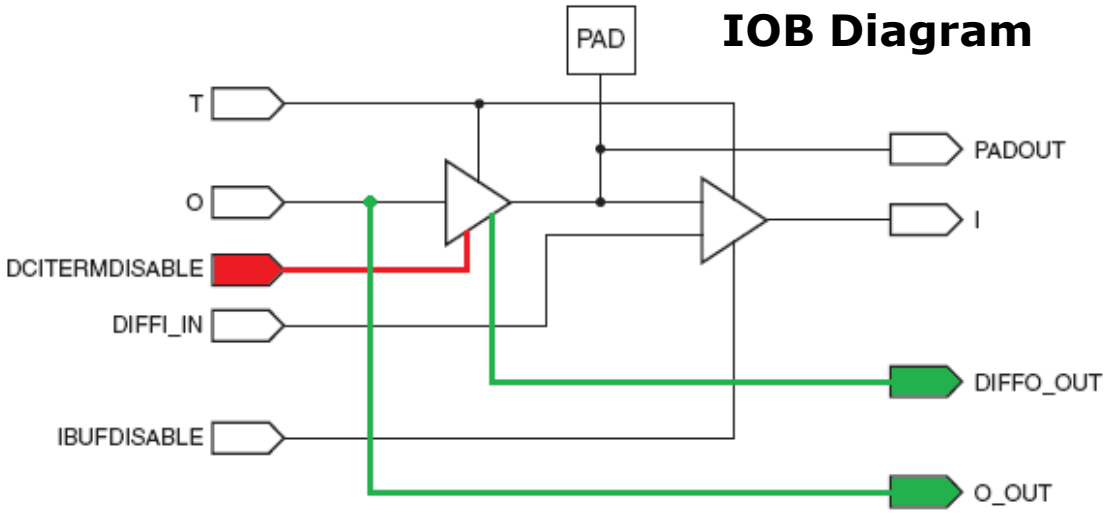


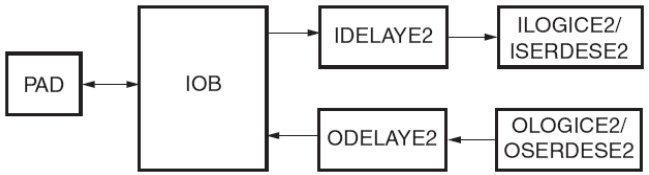
Xilinx Artix-7
GTP Transceivers



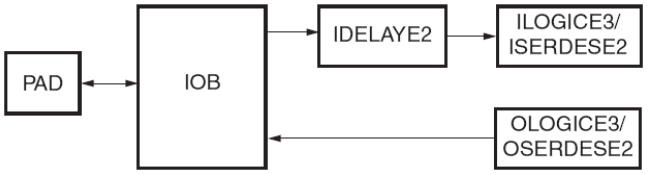


Input / Output Tiles: HR/HP





7 Series FPGA **HP** Bank I/O Tile
High Performance – fast signals



7 Series FPGA **HR** Bank I/O Tile
High Range – wide voltage range

Programmable:

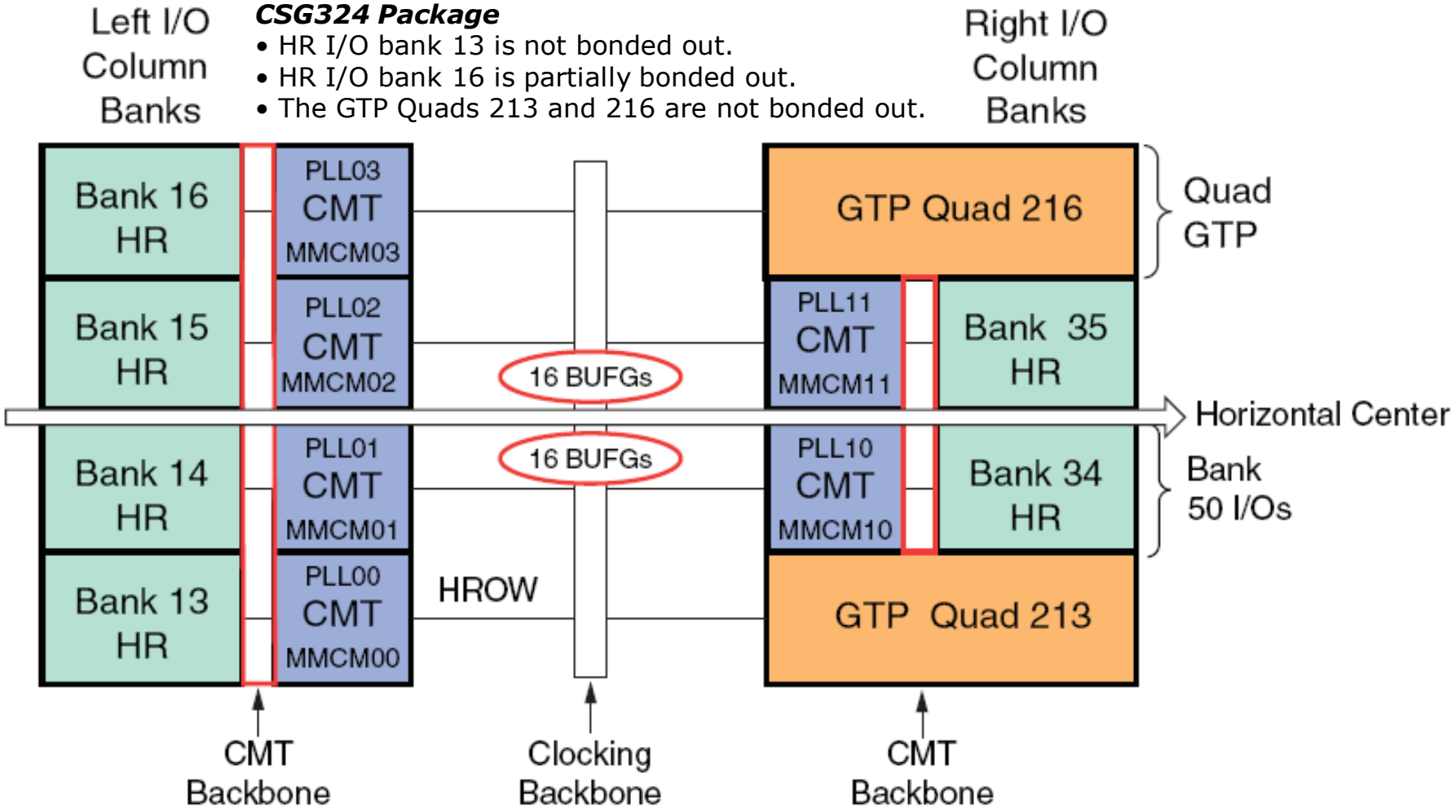
- pull-up / pull-down
- weak-keeper
- DCI (Digital Controlled Impedance)
- Output Drive Strength (2…24mA)

Single-ended:
LVCMOS, LVTTL, HSTL, PCI, SSTL

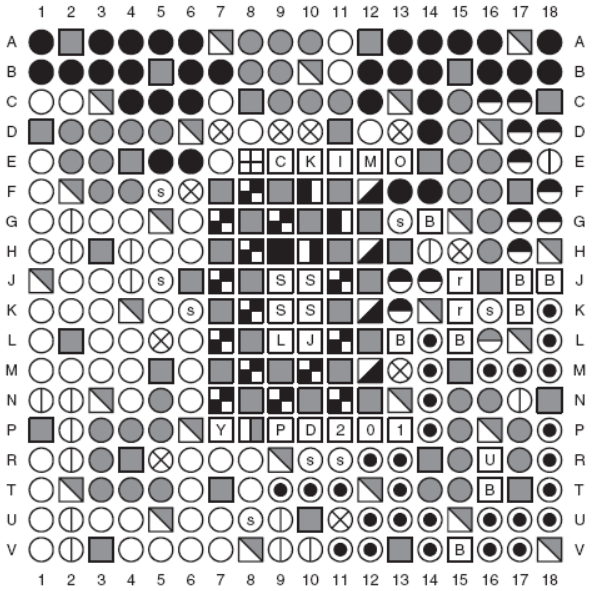
Balanced:
LVDS, MiniLVDS, RSDS, PPDS, BLVDS, diff HSTL & SSTL

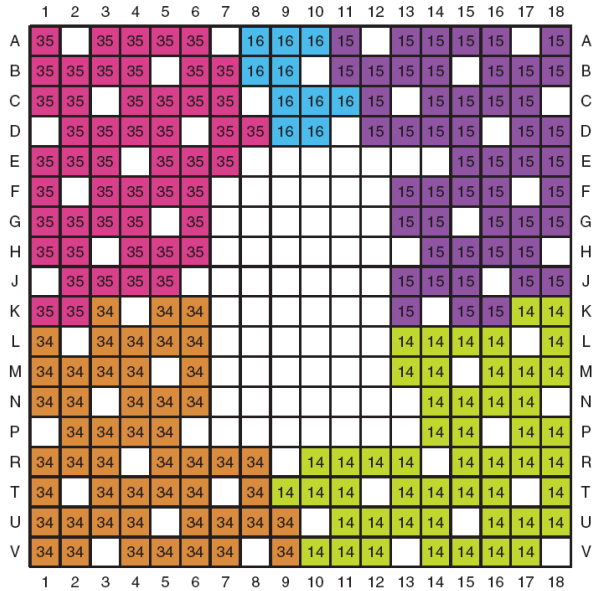
Xilinx Artix-7
SelectIO: XC7A100T-CSG324

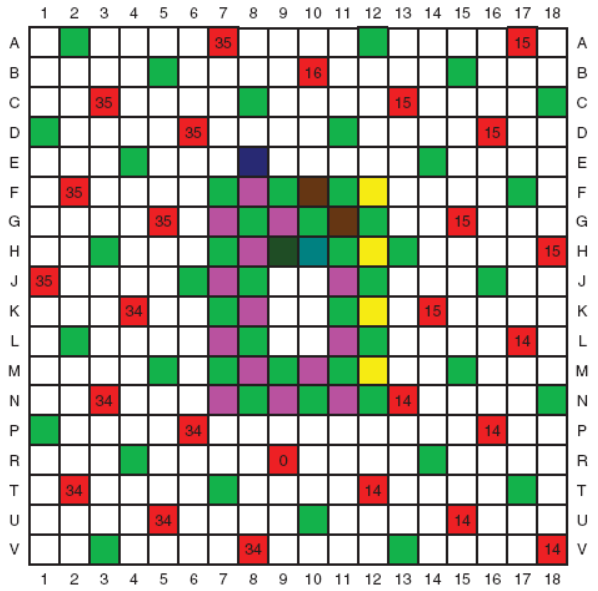
CSG324 Package
- HR I/O bank 13 is not bonded out.
- HR I/O bank 16 is partially bonded out.
- The GTP Quads 213 and 216 are not bonded out.



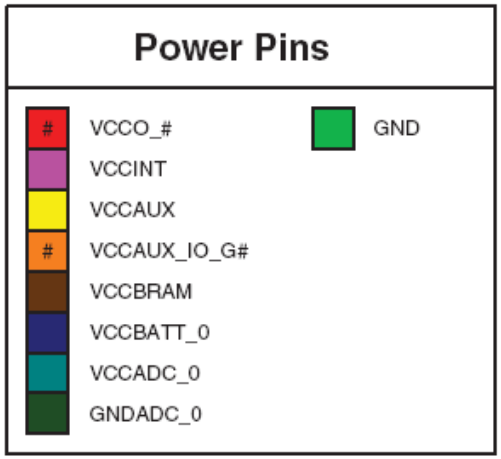
Xilinx Artix-7
XC7A100T-CSG324 Package Pins





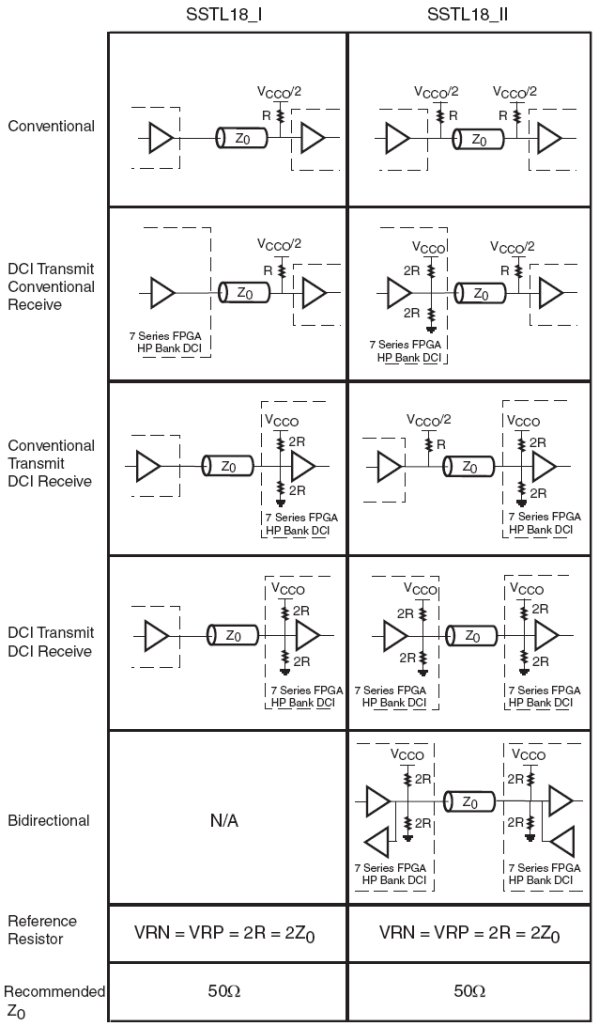


User I/O Pins	Dedicated Pins	Other Pins
IO_LXXY_#	CCLK_0	GND
IO_XX_#	CFGBVS_0	VCCAUX_IO_G#
Multi–Function Pins	DONE_0	VCCAUX
ADV_B	DXP_0	VCCINT
FCS_B	DXN_0	VCCO_#
FOE_B	GNDADC_0	VCCBRAM
MOSI	INIT_B_0	NC
FWE_B	M0_0	
DOUT_CSO_B	M1_0	
CSI_B	M2_0	
PUDC_B	PROGRAM_B_0	
RDWR_B	TCK_0	
RS0–RS1	TDI_0	
AD0P/AD0N–AD15P/AD15N	TDO_0	
EMCCLK	TMS_0	
VRN	VCCADC_0	
VRP	VCCBATT_0	
VREF	VP_0	
D00–D31	VN_0	
A00–A28	VREFP_0	
DQS	VREFN_0	
MRCC		
SRCC		



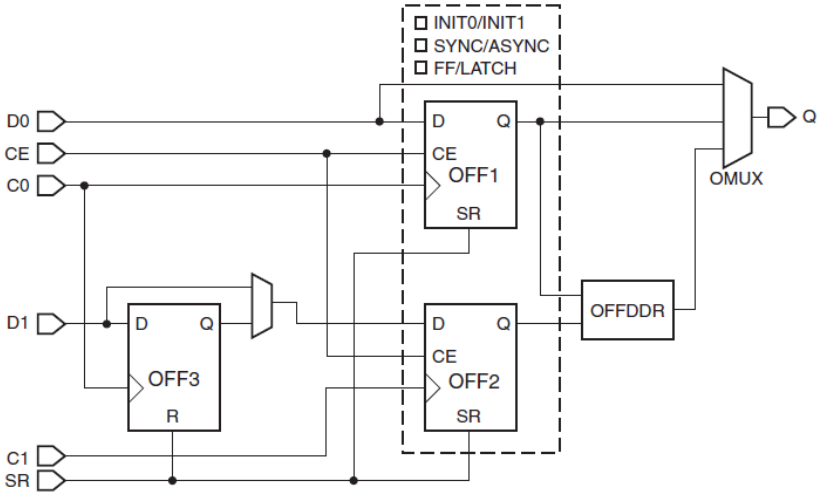
Xilinx Artix-7
SelectIO: HR/HP features, DCI option

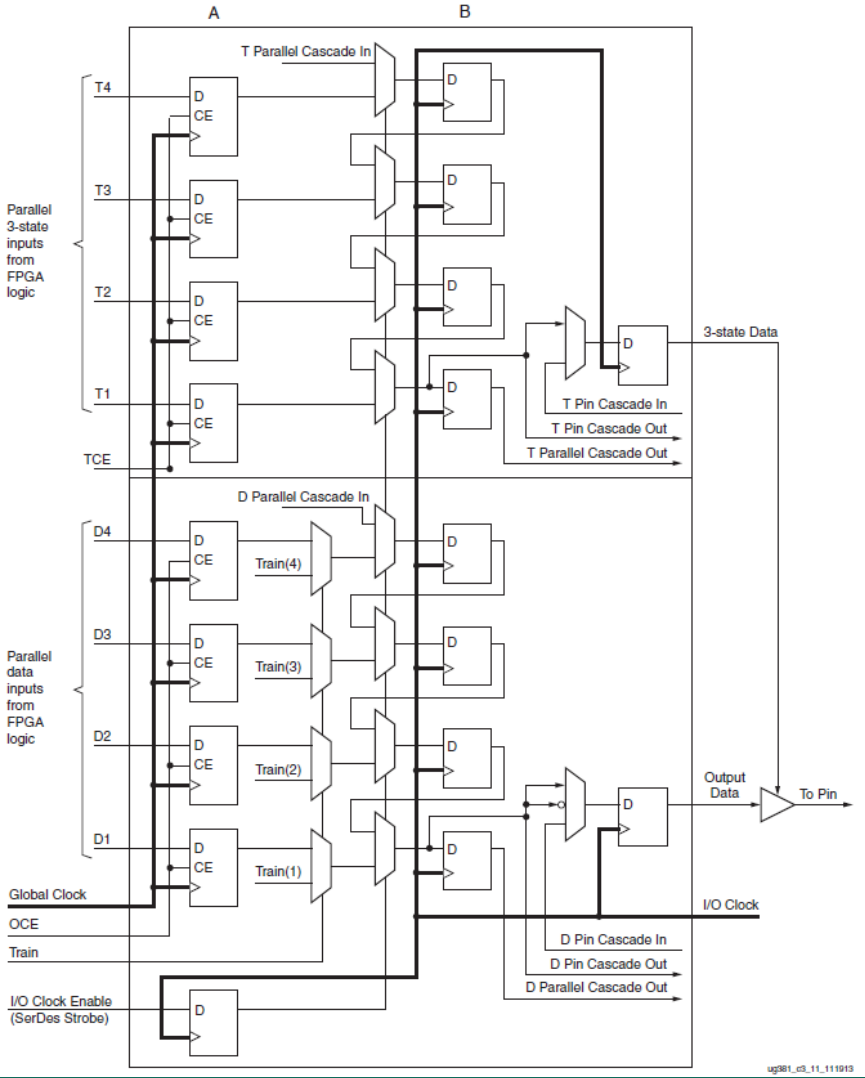
Feature	HP I/O Banks	HR I/O Banks
3.3V I/O standards(1)	N/A	Supported
2.5V I/O standards(1)	N/A	Supported
1.8V I/O standards(1)	Supported	Supported
1.5V I/O standards(1)	Supported	Supported
1.35V I/O standards(1)	Supported	Supported
1.2V I/O standards(1)	Supported	Supported
LVDS signaling	Supported(2)	Supported
24 mA drive option for LVCMOS18 and LVTTL outputs	N/A	Supported
V_{CCAUX_IO} supply rail	Supported	N/A
Digitally-controlled impedance (DCI) and DCI cascading	Supported	N/A
Internal V_{REF}	Supported	Supported
Internal differential termination (DIFF_TERM)	Supported	Supported
IDELAY	Supported	Supported
ODELAY	Supported	N/A
IDELAYCTRL	Supported	Supported
ISERDES	Supported	Supported
OSERDES	Supported	Supported
ZHOLD_DELAY	N/A	Supported



Xilinx Spartan-6
OLOGIC / OSERDES

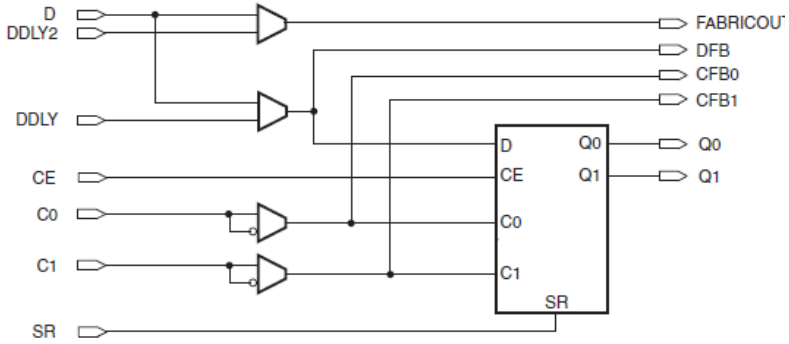
- SDR / DDR
- OFF3 – data alignment
- 2..8:1 serialization
  (5..8:1 – cascaded)
- independent Tri-State path
- training pattern

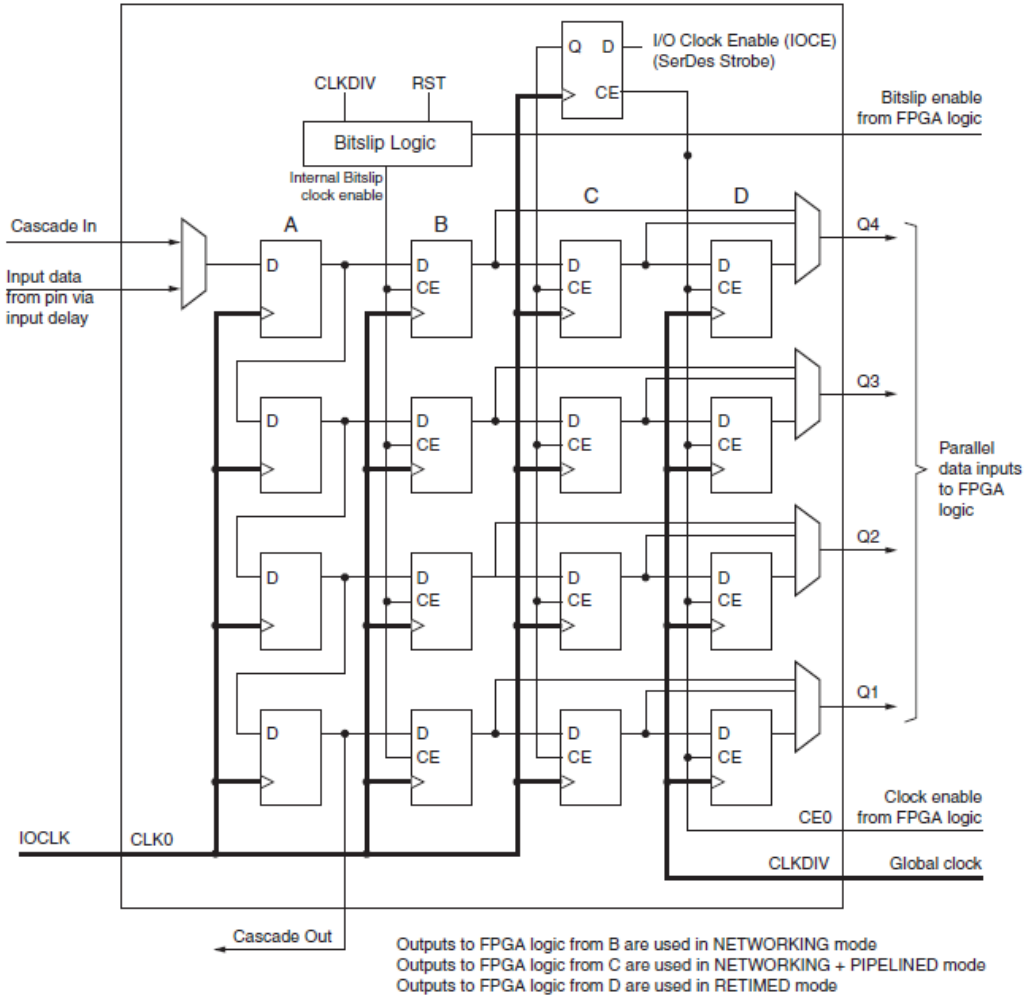




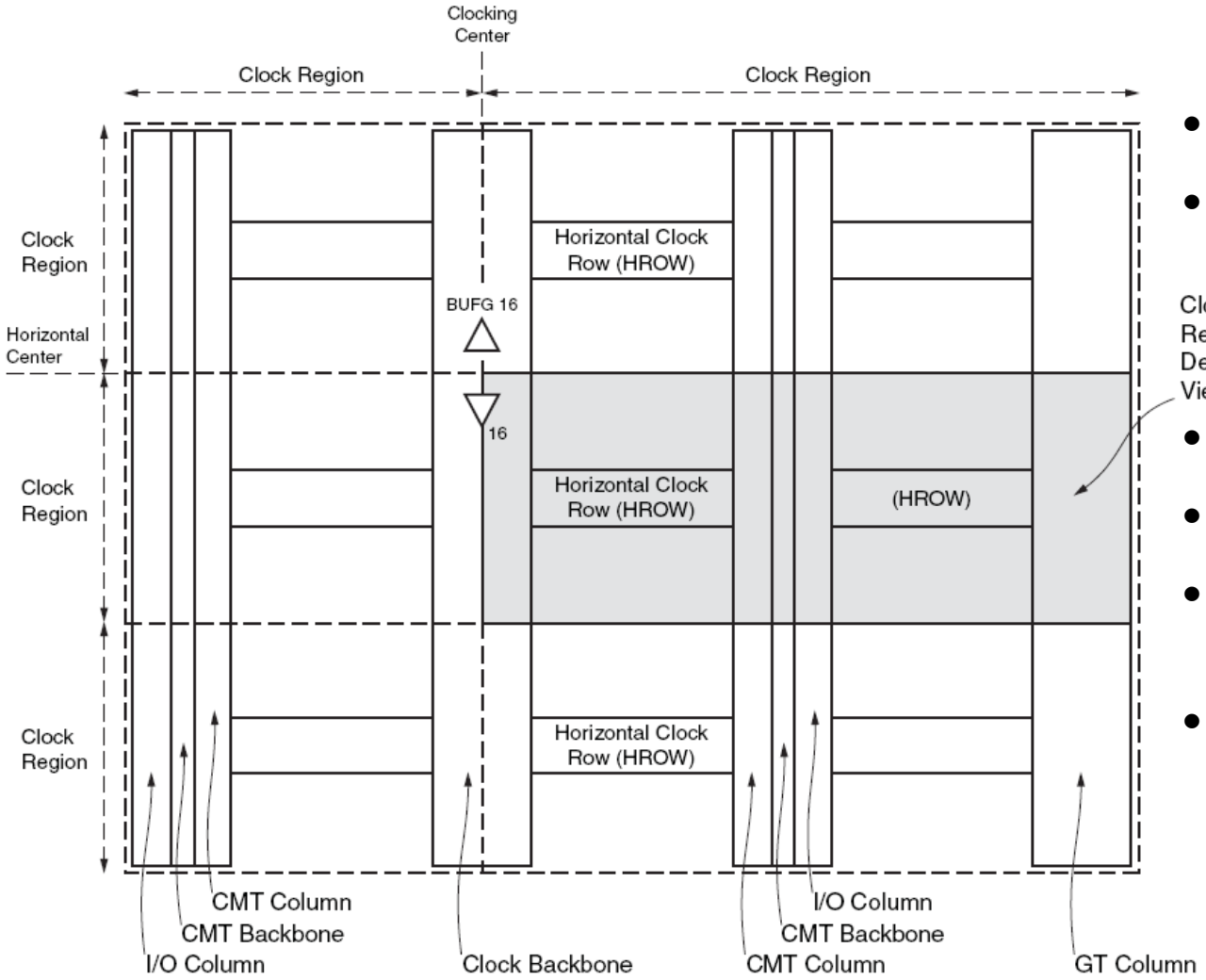
ILOGIC / ISERDES

- SDR / DDR
- 2..8:1 serialization
  (5..8:1 – cascaded)
- bit-slip
- 3 synchronization stages



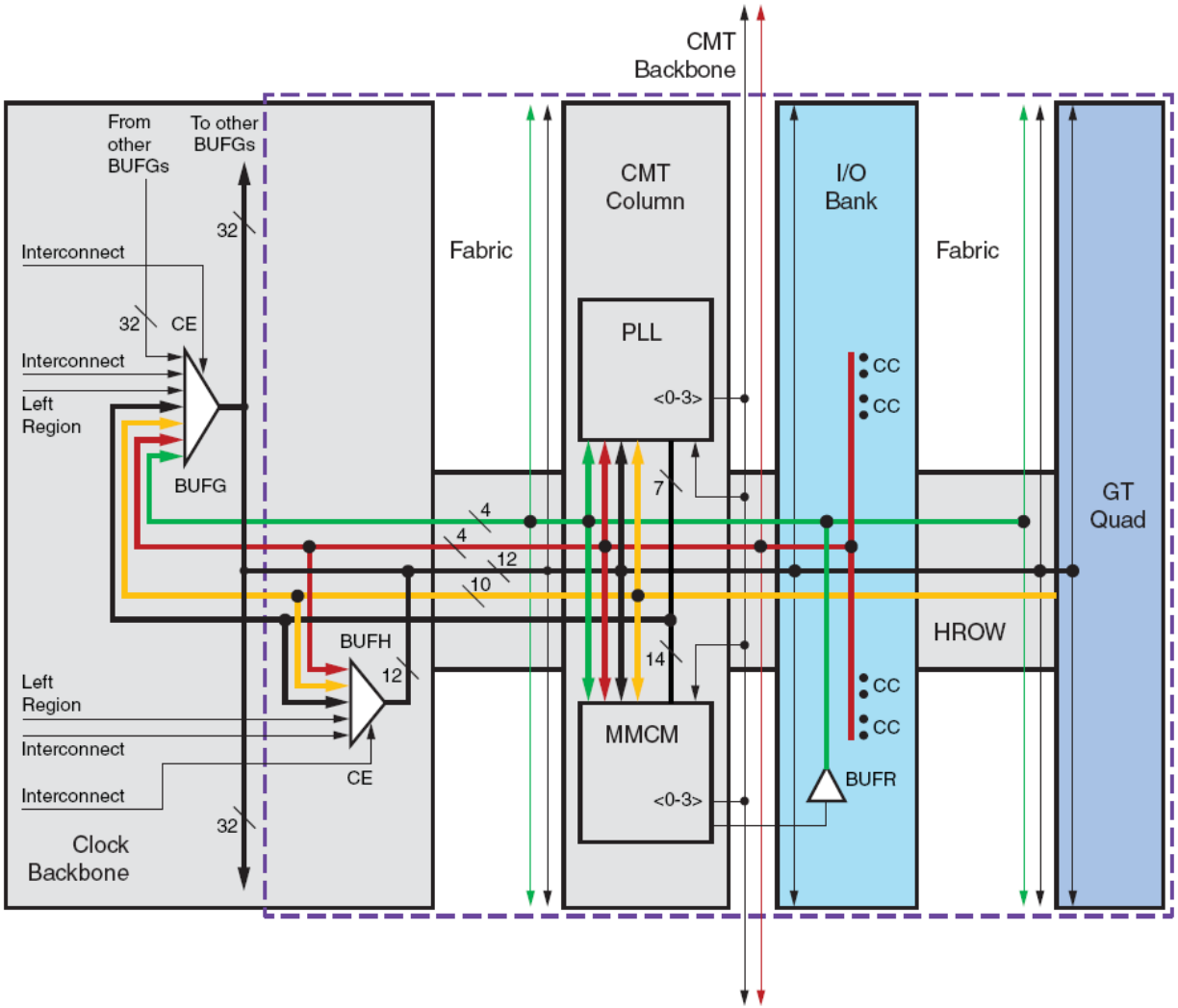


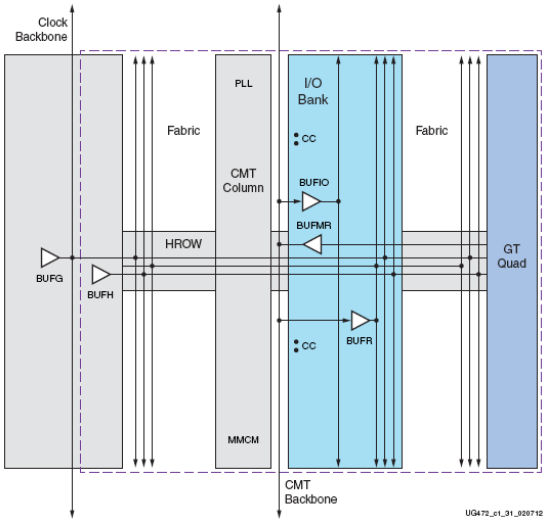
Xilinx Artix-7
Clock resources

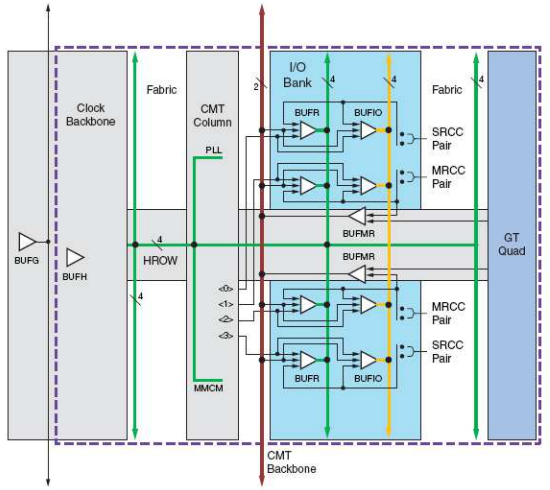


- **1…24 Clock Regions**
- **CR is 50 CLBs high**
- **HROW in center of CR**
- **SRCC / MRCC pins**
- **Clock Management Tiles**
- **Buffers: BUFIO, BUFR, BUFMR, BUFH, BUFG, BUFGCE, BUFGMUX**

Xilinx Artix-7
Clock resources

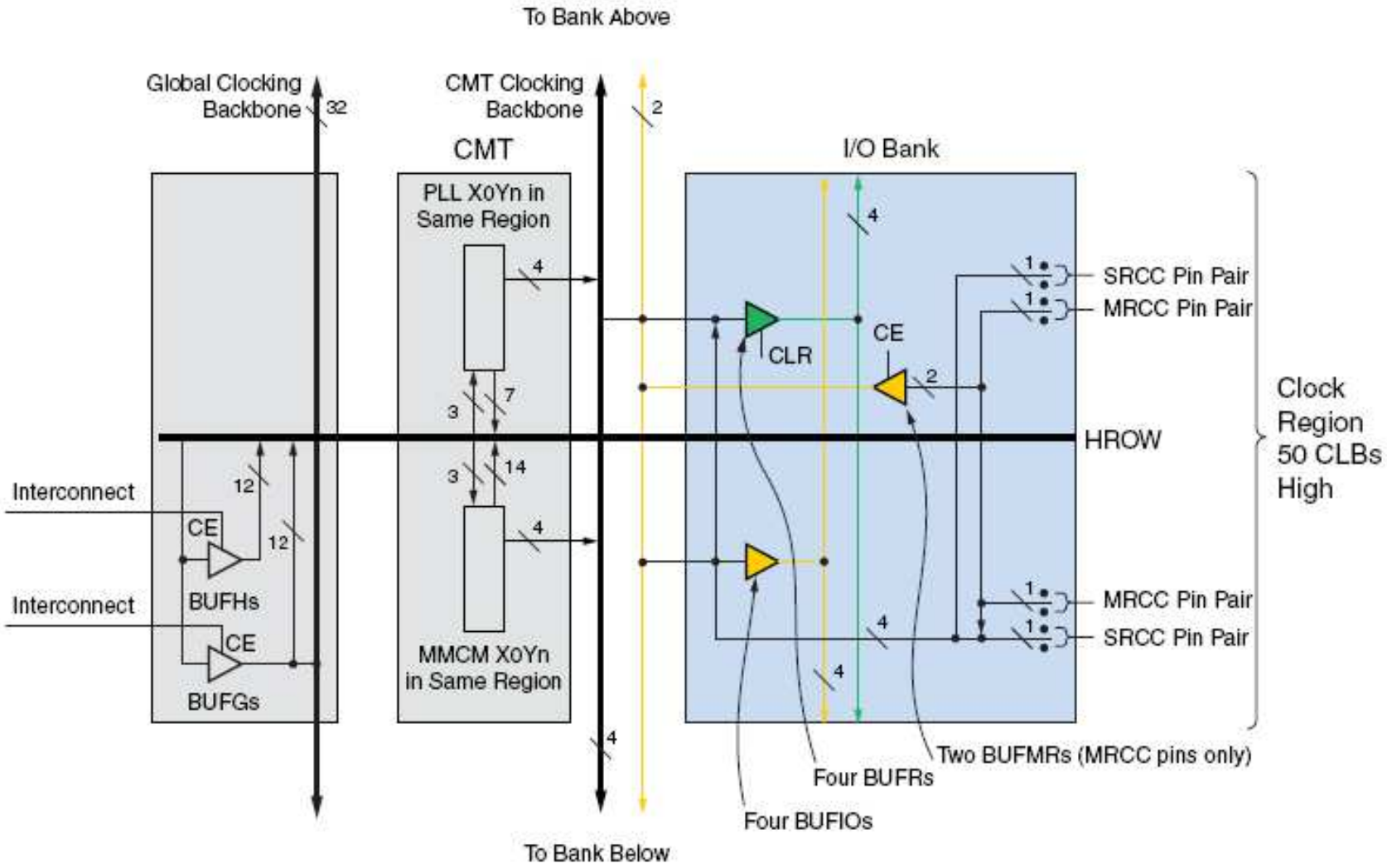






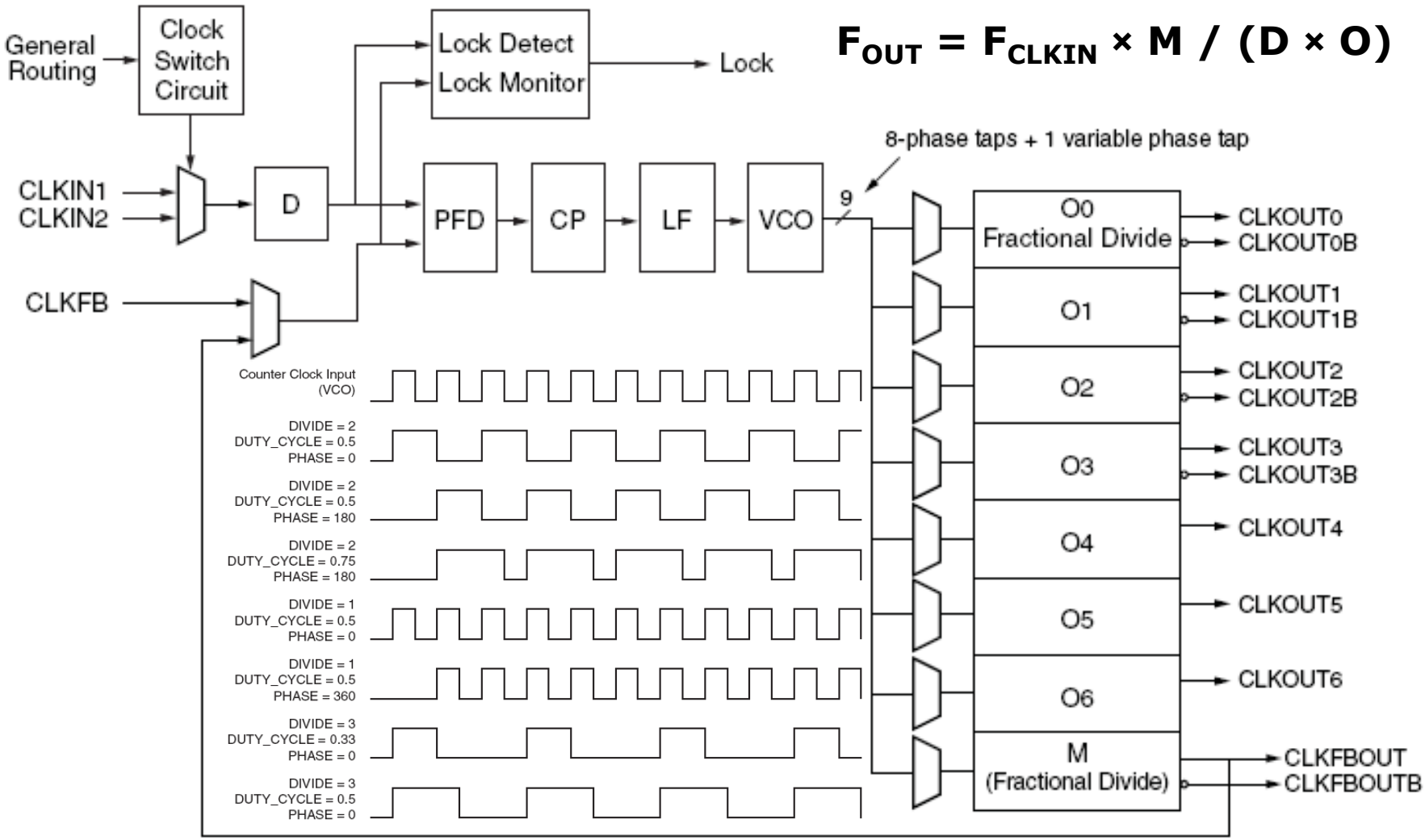
Clock Management Tile

Phase Locked Loop + Mixed-Mode Clock Manager



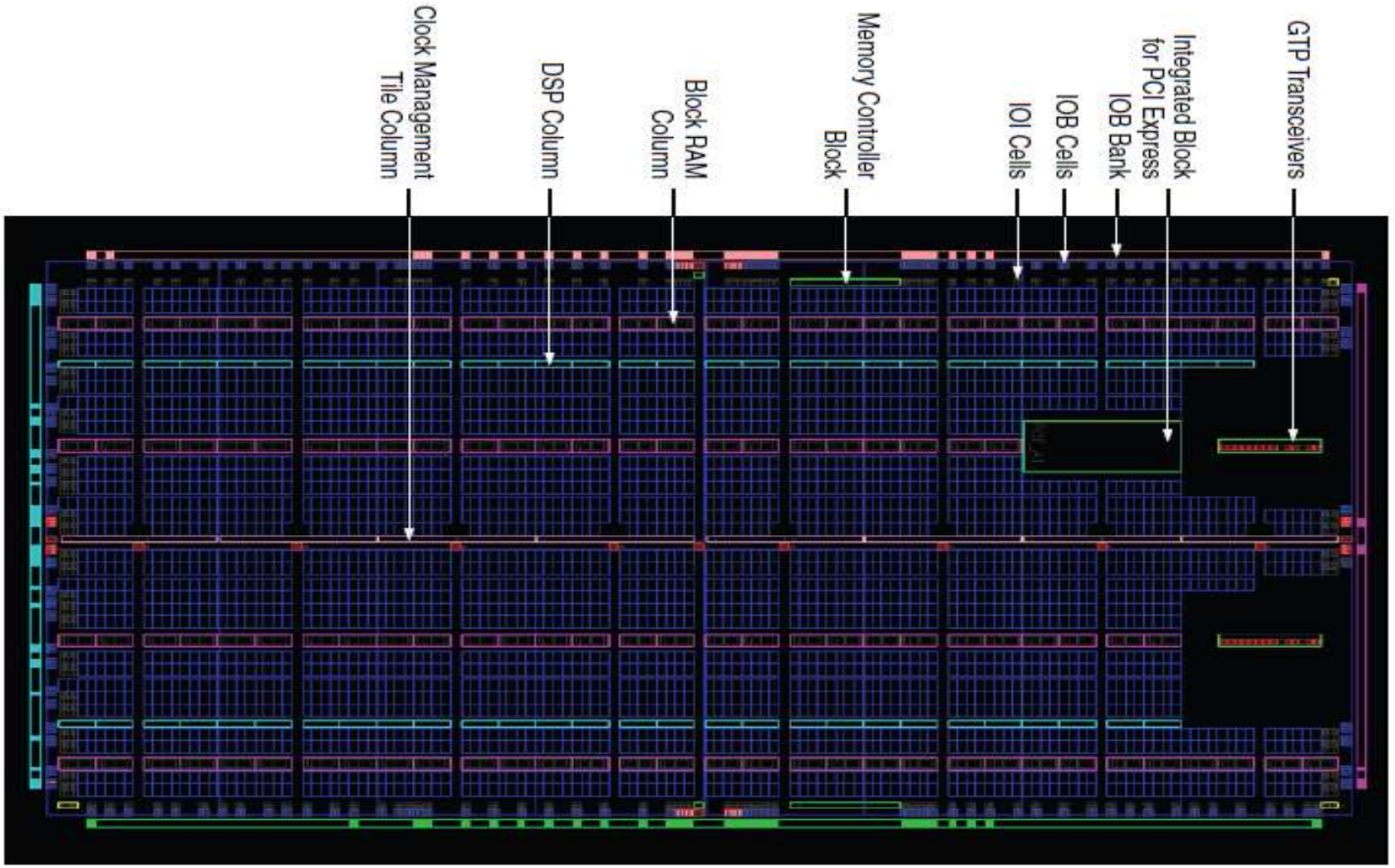
Clock Management Tile

Mixed-Mode Clock Manager

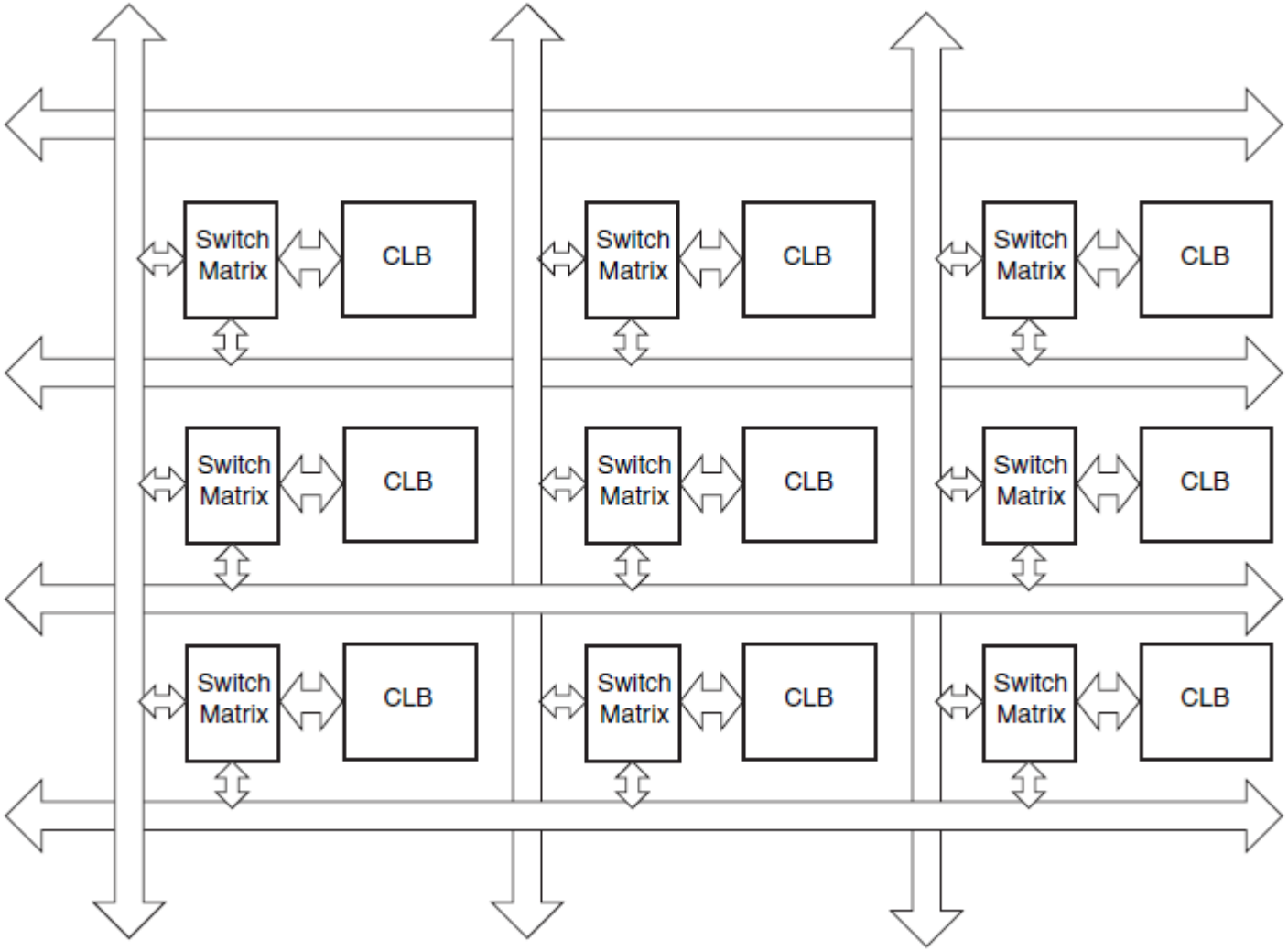


$$F_{OUT} = F_{CLKIN} \times M / (D \times O)$$

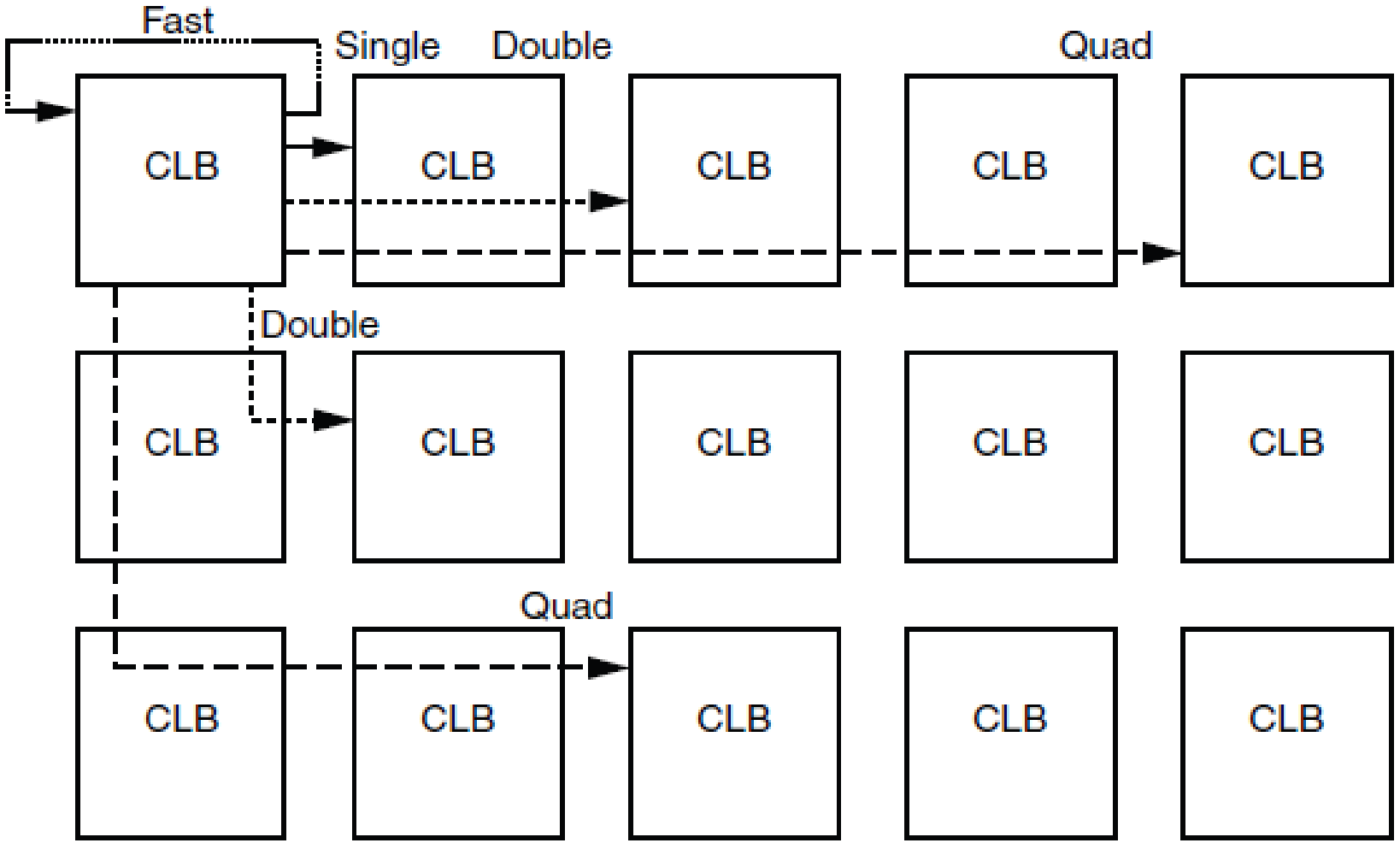
Xilinx Spartan-6
Floorplan



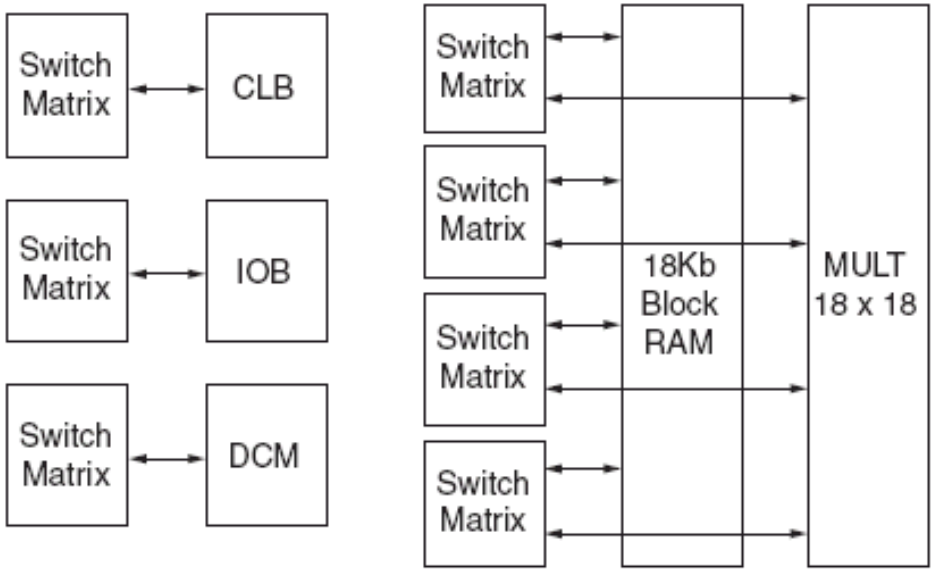
Xilinx Spartan-6
Interconnect resources

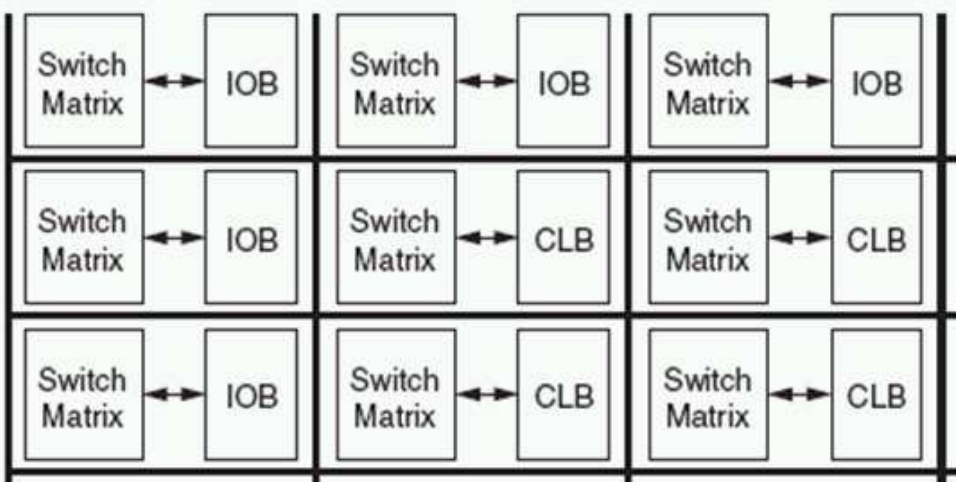


Interconnect resources



Interconnect resources



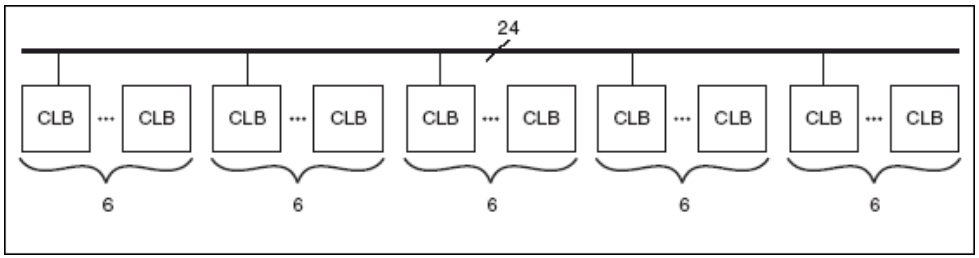


Interconnect Tile:
Switch Matrix connected with functional block
(CLB, IOB, DCM, BRAM, MULT)

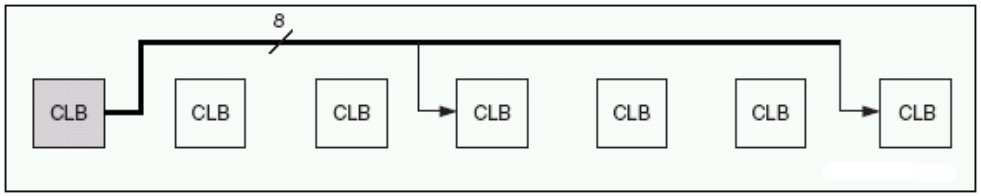
Connections:

- ***long lines***
- ***hex lines***
- ***double lines***
- ***direct lines***

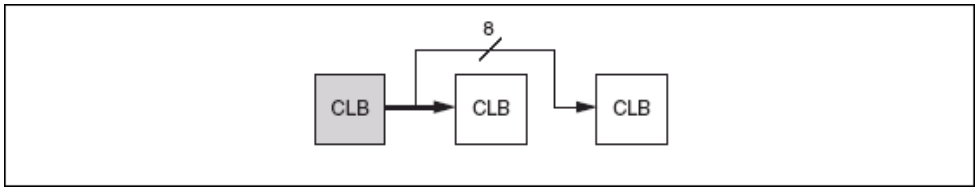
Xilinx Spartan-3
Interconnect resources



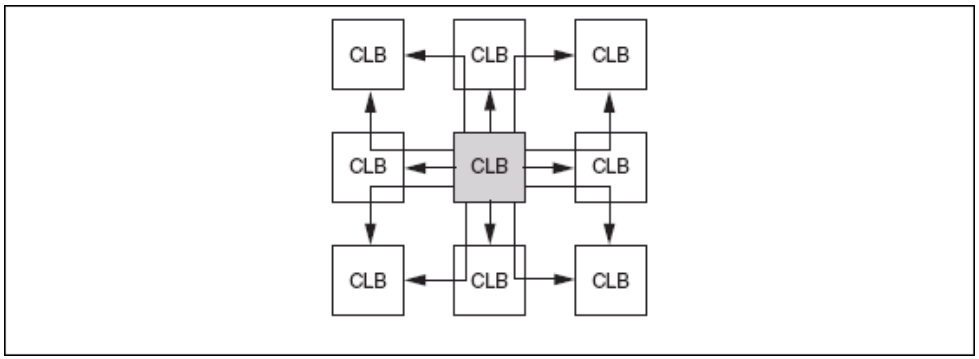
- 24 vertical & horizonatal long lines per each column/row,
- running through whole device
- tapped every 6 Switch Matrices



- 8 hex lines in 4 directions
- driver on one end, receiver in the middle & on the other end
- tapped every 3 Switch Matrices



- 8 double lines in 4 directions
- driver on one end, receiver in the middle & on the other end

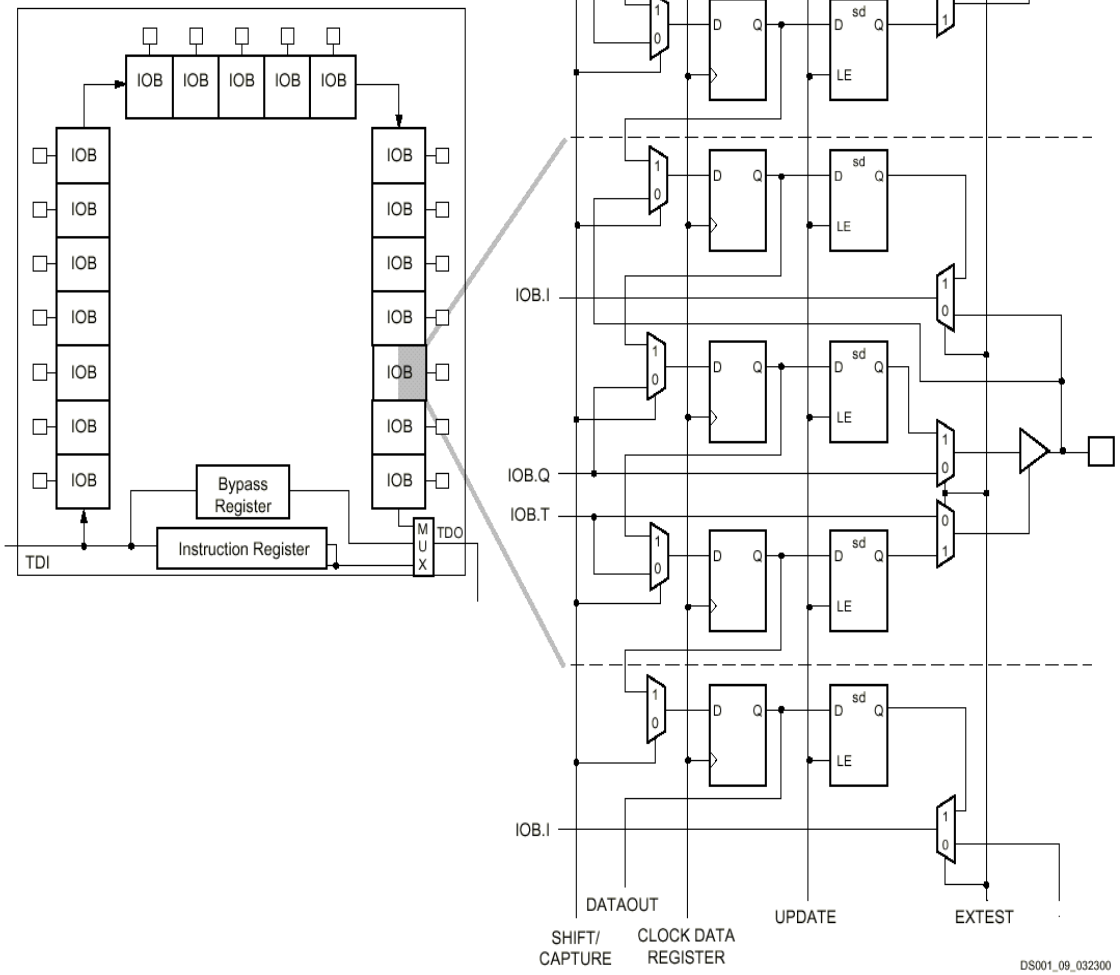


- direct lines in 8 directions
- nearest neighbours connections

Configuration modes:

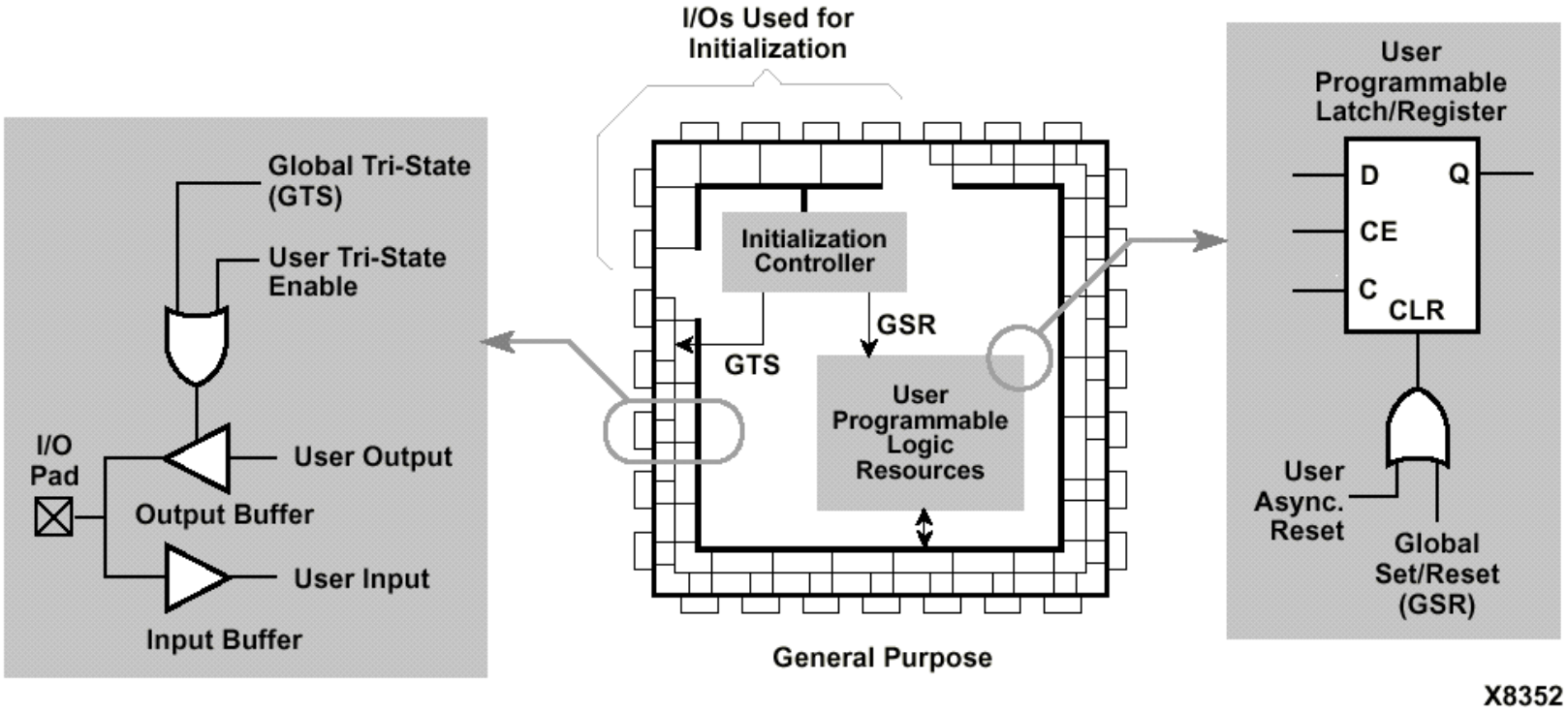
- **Slave Serial**
- **Master Serial**
- **Slave Parallel (SelectMAP)**
- **Boundary Scan (JTAG)**

***ReadBack*:**
verification of configuration memory, flip-flops states and memories contents (debug)



GSR i GTS global signals

- GSR – Global Set/Reset
- GTS – Global Tri-State

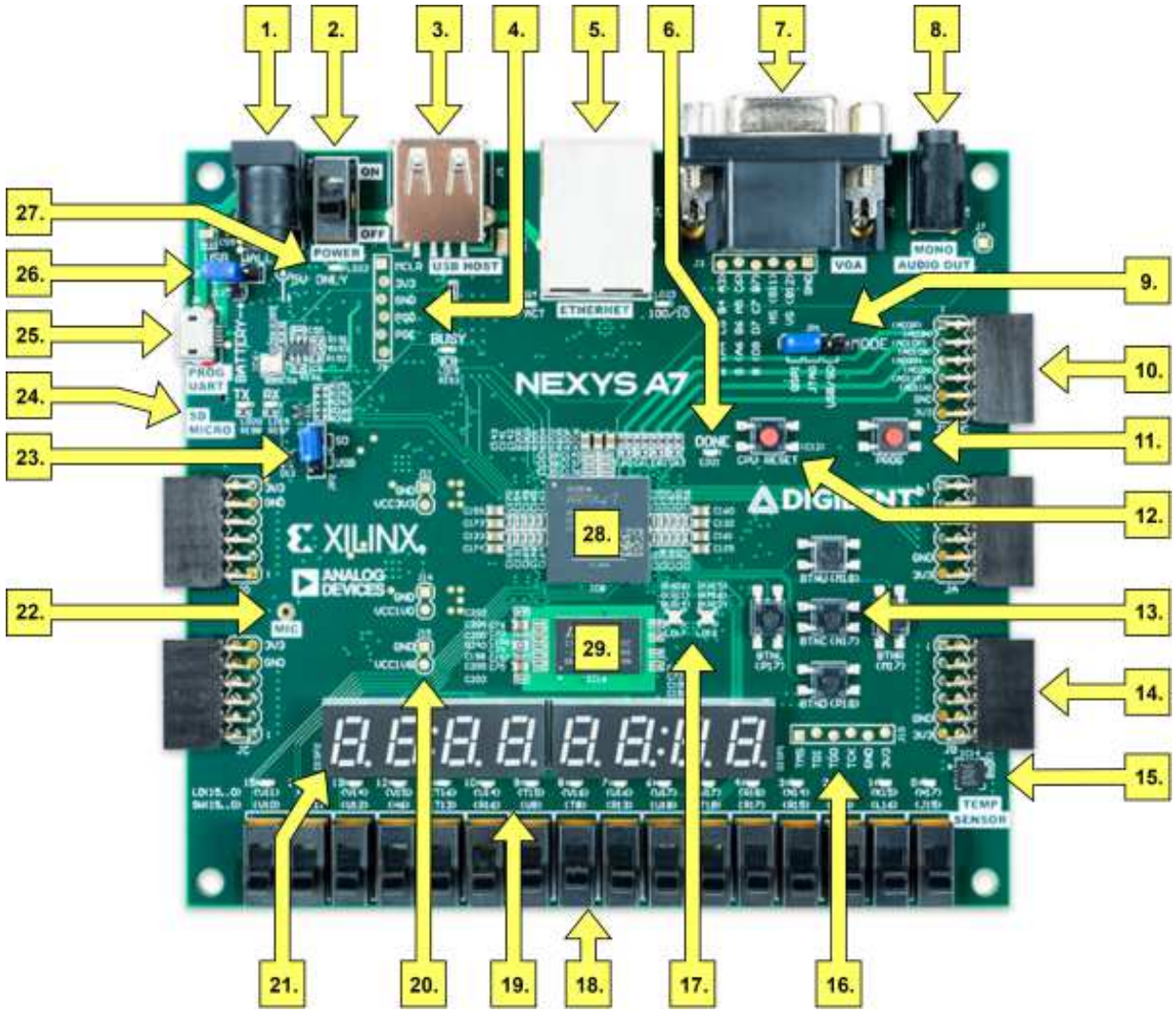


FPGA Resources

XC7A100T-1CSG324C device:

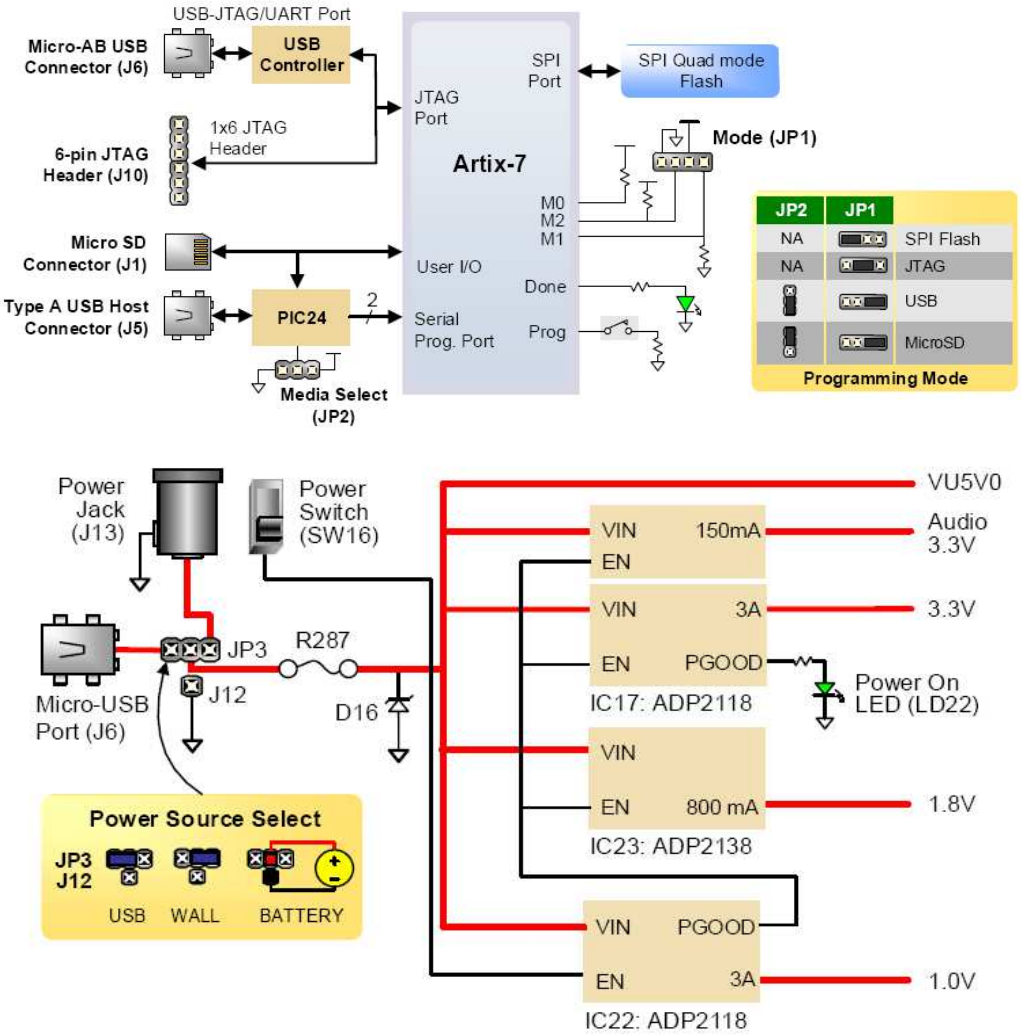
- **15,850 Logic Slices:**
  - **64,400 LUTs**
  - **101,440 Logic Cells**
  - **128,800 Flip-Flops**
- **1,188Kb distributed memory**
- **4,860Kb block memory in 135 blocks**
- **240 DSP48E1 blocks**
- **6 CMT blocks**
- **210 user I/Os in 6 banks**

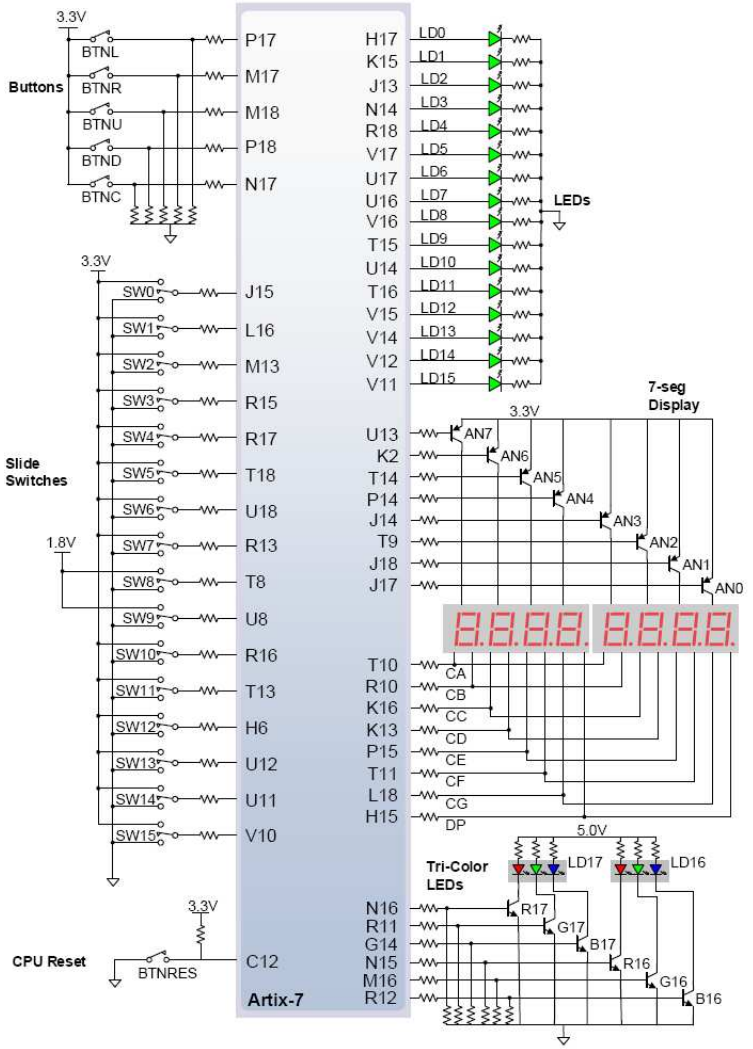
Digilent Nexys™4 DDR (Nexys A7) FPGA Board
PCB Resources



1 Power jack
2 Power switch
3 USB host connector
4 PIC24 programming port (factory use)
5 Ethernet connector
6 FPGA programming done LED
7 VGA connector
8 Audio connector
9 Programming mode jumper
10 Analog signal Pmod port (XADC)
11 FPGA configuration reset button
12 CPU reset button (for soft cores)
13 Five pushbuttons
14 Pmod port(s)
15 Temperature sensor
16 JTAG port for (optional) external cable
17 Tri-color (RGB) LEDs
18 Slide switches (16)
19 LEDs (16)
20 Power supply test point(s)
21 Eight digit 7-seg display
22 Microphone
23 External configuration jumper (SD/USB)
24 MicroSD card slot
25 Shared UART/ JTAG USB port
26 Power select jumper and battery header
27 Power-good LED
28 Xilinx Artix-7 FPGA
29 DDR2 memory

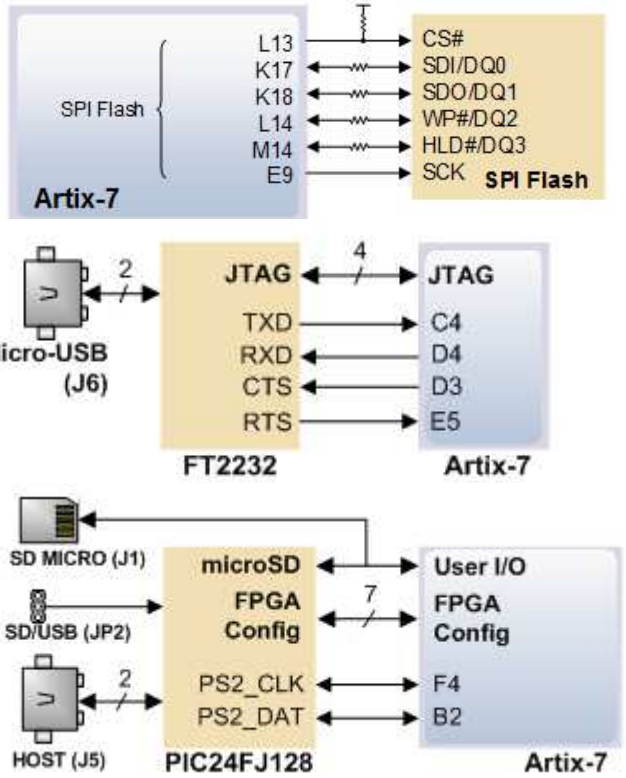
Digilent Nexys™4 DDR (Nexys A7) FPGA Board
PCB resources

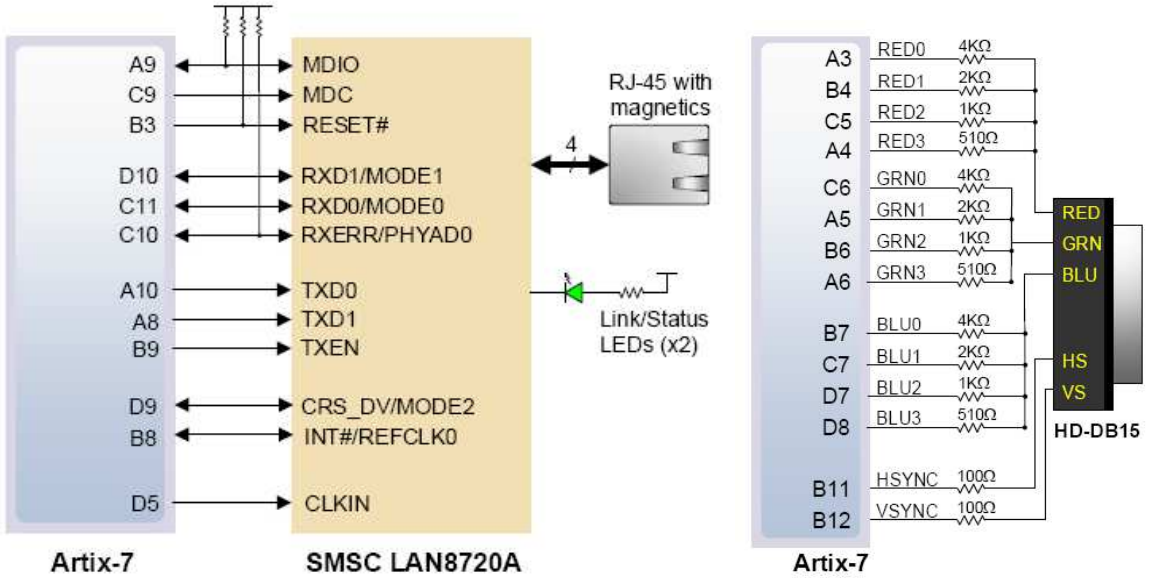


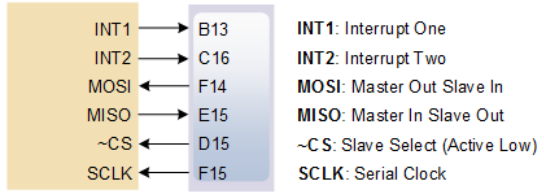


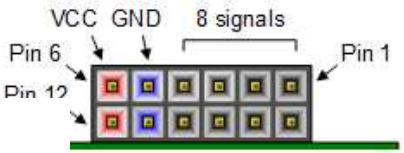
Digilent Nexys™4 DDR (Nexys A7) FPGA Board
PCB resources

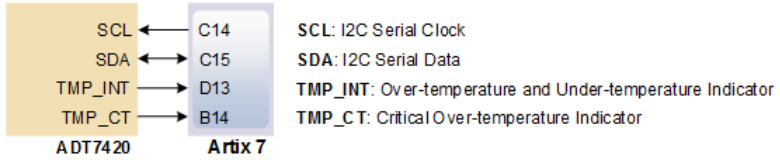
Setting	Value
Memory type	DDR2 SDRAM
Max. clock period	3000ps (667Mbps data rate)
Recommended clock period (for easy clock generation)	3077ps (650Mbps data rate)
Memory part	MT47H64M16HR-25E
Data width	16
Data mask	Enabled
Chip Select pin	Enabled
Rtt (nominal) – On-die termination	50ohms
Internal Vref	Enabled
Internal termination impedance	50ohms












To be continued…