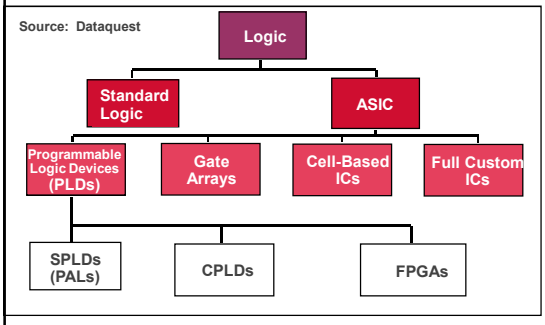
SPLD & CPLD architectures

PLD devices classification



Configurable Logic Blocks (CLB)
- *Memory Look-Up Table*
- *AND-OR planes*
- *Simple gates*

Input / Output Blocks (IOB)
- *Bidirectional, latches, inverters,*
- *pullup/pulldowns*

Interconnect or Routing
- *Local, internal feedback, and global*

SPLD = Simple Prog. Logic Device
PAL = Programmable Array of Logic
CPLD = Complex PLD
FPGA = Field Prog. Gate Array

ISP –In System Programmable

Agenda

- Programmable Logic Devices classification
- Simple Programmable Logic Devices (SPLD)
  - *History & backgroud,*
  - *PAL , GAL devices*
- Complex Programmable Logic Devices (CPLD)
  - *Lattice, Altera(Intel), Xilinx examples*
- CPLD applications

References

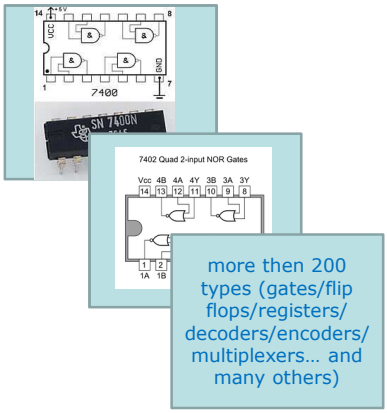
- WWW SPLD, CPLD manufactures
  - www.altera.com (Intel from June 2017)

    (Intel is paying $16.7 billion in an all-cash deal to buy smaller peer Altera, the second major acquisition in the semiconductor sector in less than a week)
  - www.atmel.com
  - www.latticesemi.com
  - www.xilinx.com
- EDA pages like
  - http://www.eetimes.com/design/programmable-logic

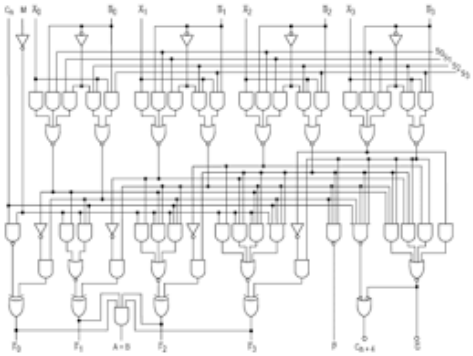
1970..80 – digital world before PLD (standard logic)

TEXAS INSTRUMENTS

1961 TTL series 7400, CMOS series 4000



more then 200 types (gates/flip flops/registers/ decoders/encoders/ multiplexers… and many others)



SPLD – *Simple Programmable Logic Devices*

- PAL (*Programmable Array Logic, AMD Vantis*)
- PLA (*Programmable Logic Array*)
- GAL (*Generic Array Logic, Lattice*)

Advanced Micro Devices

VANTIS

ATMEL Everywhere You Are®

CYPRESS PERFORM

Lattice Semiconductor Corporation

TEXAS INSTRUMENTS

Canonical form

Sum-of-products canonical forms

- Also known as disjunctive normal form
- Also known as minterm expansion

F = *001* *011* *101* *110* *111*

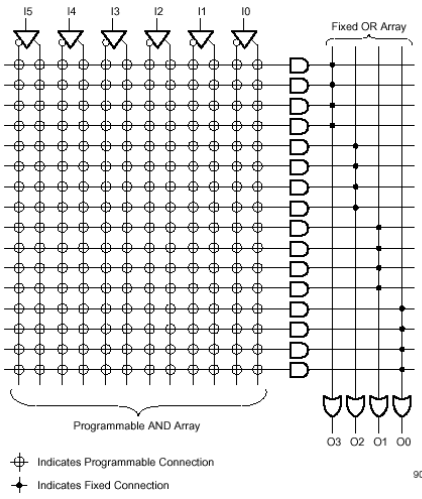
F = A′B′C + A′BC + AB′C + ABC′ + ABC

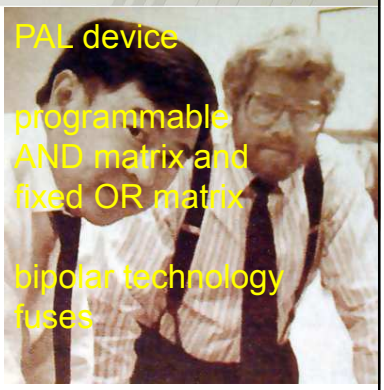
A	B	C	F	F′
0	0	0	0	1
0	0	1	1	0
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	0

F′ = A′B′C′ + A′BC′ + AB′C′

http://www.cs.ucr.edu/~ehwang/courses/cs120a/minterms.pdf

PAL device basic structure

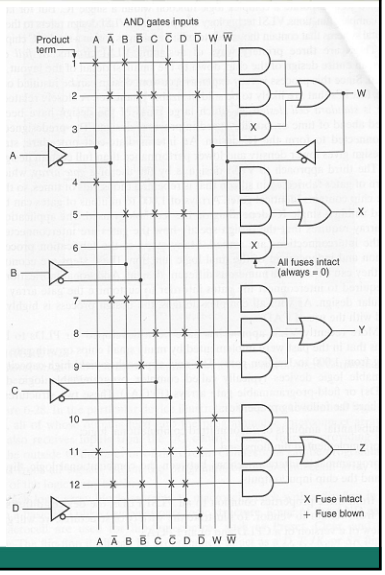




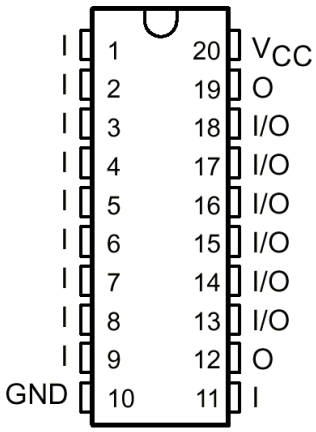
John Birkner and H.T. Chua of Monolithic Memories worked with Andy Chan to introduce a more streamlined architecture they called Programmable Array Logic (PAL) in 1978

PAL device – logic function example

Product term	AND Inputs A	B	C	D	W	Outputs
1	1	1	0	—	—	$W = A\bar{B}\bar{C}$
2	0	0	1	0	—	$+\bar{A}\bar{B}CD$
3	—	—	—	—	—	
4	1	—	—	—	—	$X = A$
5	—	1	1	1	—	$+BCD$
6	—	—	—	—	—	
7	0	1	—	—	—	$Y = \bar{A}B$
8	—	—	1	1	—	$+CD$
9	—	0	—	0	—	$+\bar{B}\bar{D}$
10	—	—	—	—	1	$Z = W$
11	1	—	0	0	—	$+A\bar{C}\bar{D}$
12	0	0	0	1	—	$+\bar{A}\bar{B}\bar{C}\bar{D}$



Simple PLD

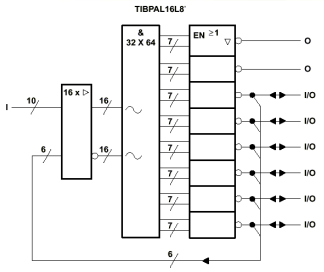


- **PAL**
  (***Programmable Array Logic***)
  16L8, 16R4, 16R6, 16R8

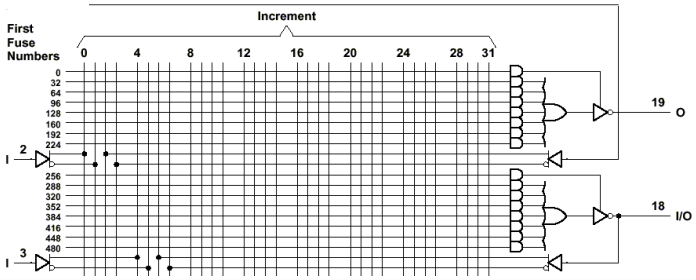
- **GAL**
  (***Generic Array Logic***)
  16V8, 20V8, 22V10, 26V12

- **PLA**
  (***Programmable Logic Array***)

Simple PLD– PAL16L8



Block diagram and internal architecture



PAL devices - families 12,14,16,20

Bipolar technology
One time programmable by „fuse” burning

Symbol

PAL xx Y z

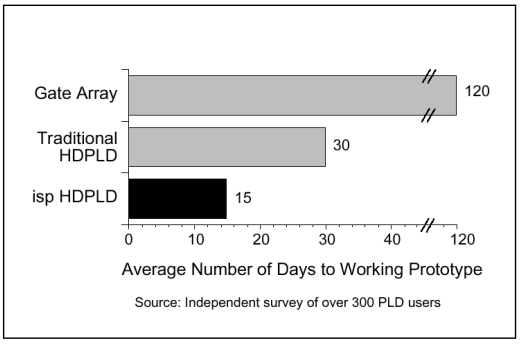
xx – inputs count
Y - L – ”low active logic”
H – ”high active logic”
C – „complemetary logic”
R synchronous flip flops
RA asynchronous flip flops
X, A extra arithmetic circuitry
S shared terms version

z - outputs count (registered or combinatorial)

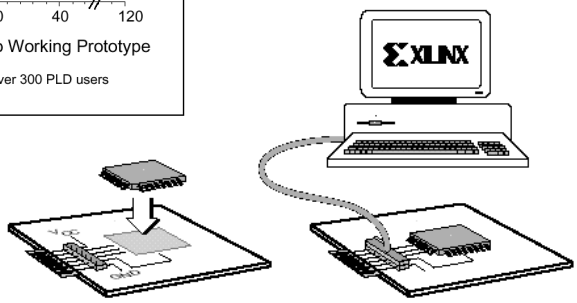
GAL - Generic Array Logic devices

Year 1985
Technology E^2CMOS
Many times (~10k and more...) programmable
Clearing time ~100ms
GAL16V8 GAL 20V10 - world wide standard

GAL ISP (*In System Programmable*)

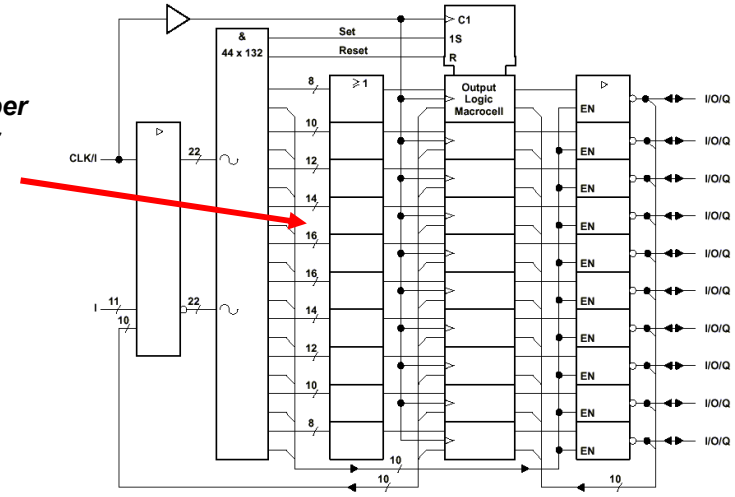


HDPLD –
High Density PLD

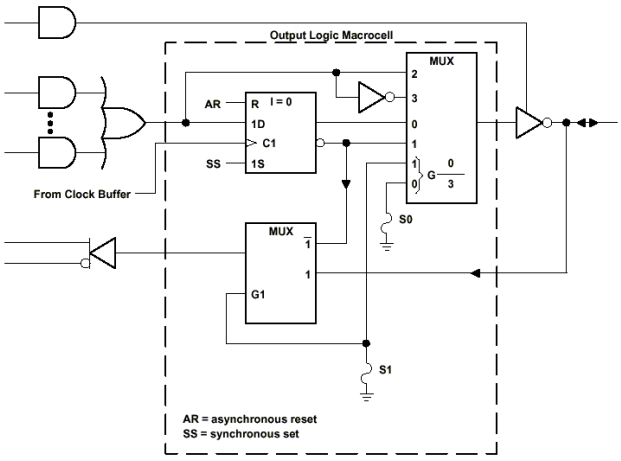


Simple PLD – GAL22V10 example

GAL devices „term" number not equal for each pin



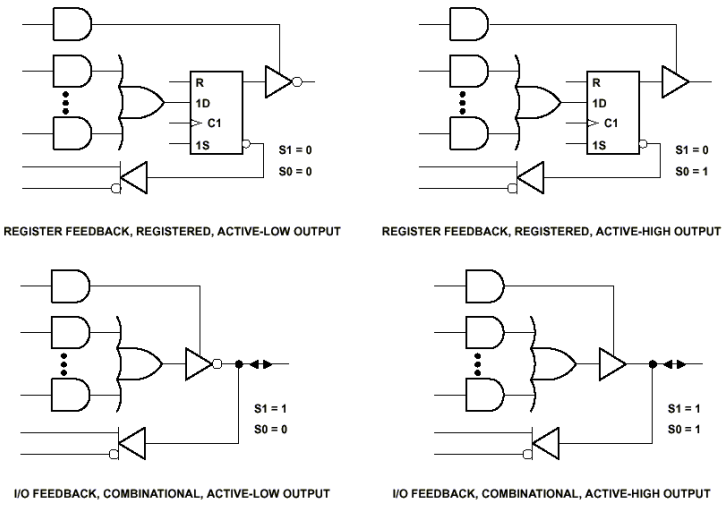
Simple PLD – GAL22V10



GAL 22V10 D flip flop inputs:

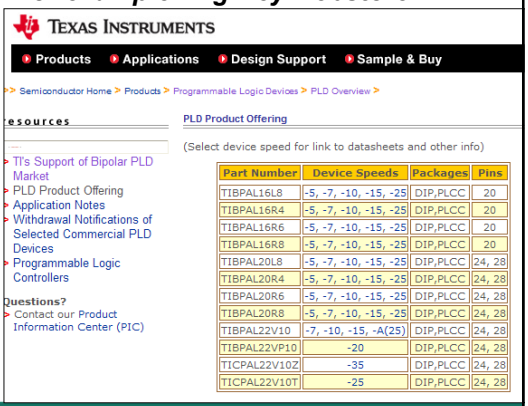
Asynchronic Reset (AR) Synchronic Set (SR)

GAL22V10 macrocell



SPLD – still on the market

Companies: Atmel, Texas Instruments
2017 –
Ready to buy SPLD
for example DigiKey webstore



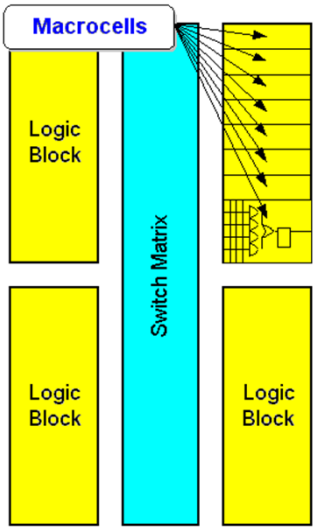
CPLD general architecture

CPLD

Macrocells (PAL like)
Commutation matrices

Technology:CMOS
(Re)Configuration:
EPROM (UV + version OTP)
EEPROM FLASH (ISP)

CPLD- Predictable timing

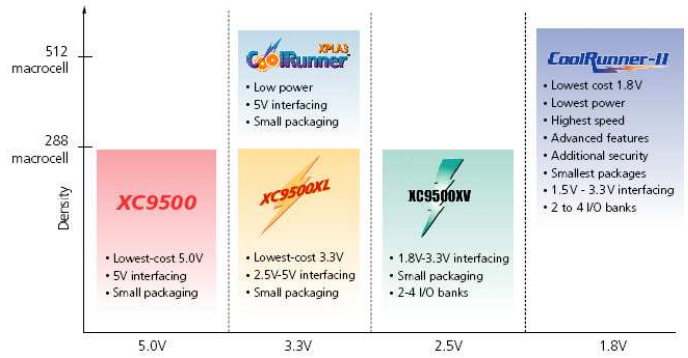


CPLD – *Complex Programmable Logic Devices*

- Altera *(CPLD leader ?)*
- Atmel *(support for older devices. 22V10 + military std)*
- Lattice *(vice leader ? CPLD..)*
- Xilinx *(CPLD as the FPGA portfolio support)*

CPLD Xilinx www.xilinx.com/cpld/

COMPLETE
CPLD SOLUTIONS.



CPLD Xilinx – XC95xx series

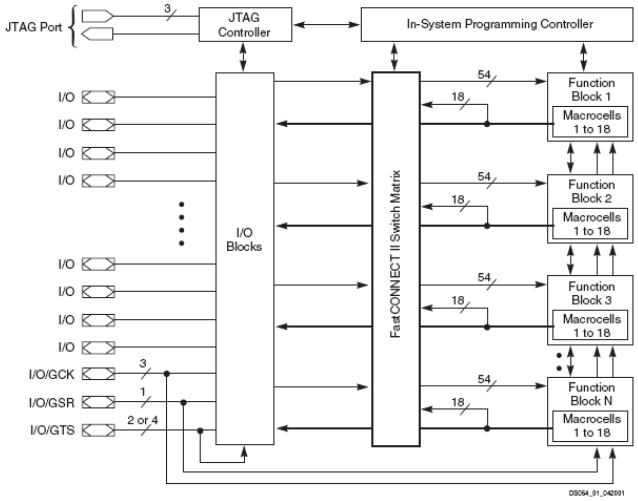


Figure 1: **XC9500XL Architecture**

CPLD Xilinx – XC95xx series

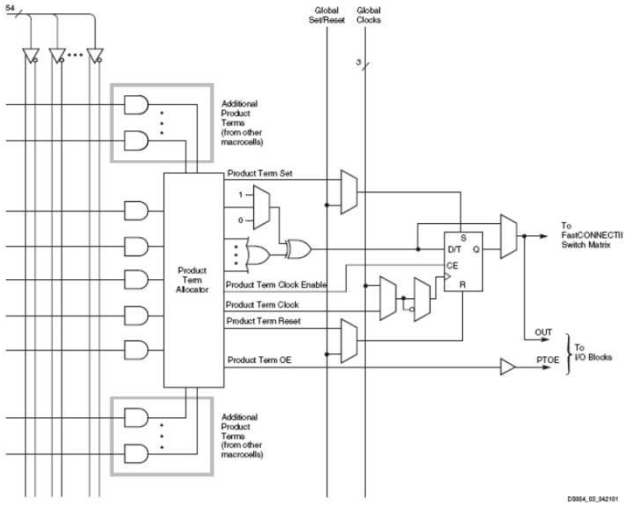


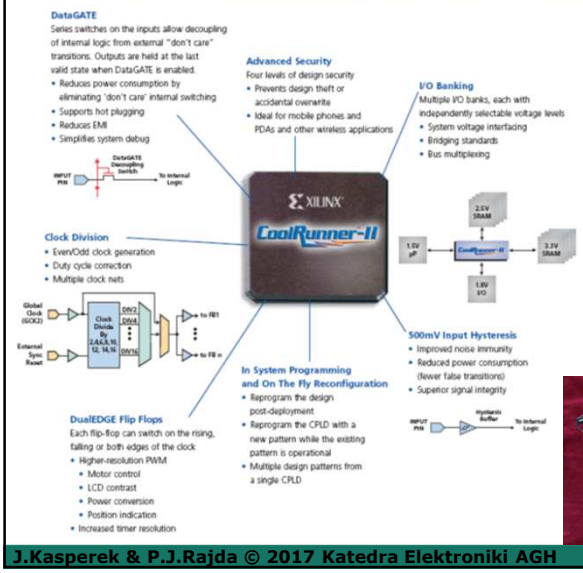
Figure 3: **XC9500XL Macrocell Within Function Block**

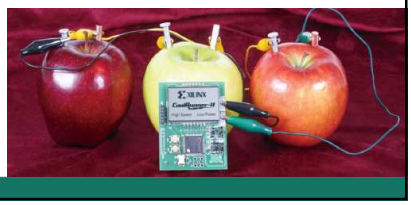
CPLD Xilinx – XC95xx series

- *Optimized for high-performance 3.3V systems*
  - *5 ns pin-to-pin logic delays, with internal system frequency up to 208 MHz*
  - *Small footprint packages including VQFPs, TQFPs and CSPs (Chip Scale Package)*
  - *Pb-free available for all packages*
  - *Lower power operation*
  - *5V tolerant I/O pins accept 5V, 3.3V, and 2.5V signals*
  - *3.3V or 2.5V output capability*
  - *Advanced 0.35 micron feature size CMOS FastFLASH technology*
- *Advanced system features*
  - *In-system programmable*
  - *Superior pin-locking and routability with FastCONNECT II™ switch matrix*
  - *Extra wide 54-input Function Blocks*
  - *Up to 90 product-terms per macrocell with individual product-term allocation*
  - *Local clock inversion with three global and one product-term clocks*
  - *Individual output enable per output pin with local inversion*
  - *Input hysteresis on all user and boundary-scan pin inputs*
  - *Bus-hold circuitry on all user pin inputs*
  - *Supports hot-plugging capability*
  - *Full IEEE Standard 1149.1 boundary-scan (JTAG) support on all devices*
- *Four pin-compatible device densities*
  - *36 to 288 macrocells, with 800 to 6400 usable gates*
  - *Fast concurrent programming*
  - *Slew rate control on individual outputs*
  - *Enhanced data security features*
- *Excellent quality and reliability*
  - *10,000 program/erase cycles endurance rating*
  - *20 year data retention*
- *Pin-compatible with 5V core XC9500 family in common package footprints*

	XC9536XL	XC9572XL	XC95144XL	XC95288XL
Macrocells	36	72	144	288
Usable Gates	800	1,600	3,200	6,400
Registers	36	72	144	288
T_{PD} (ns)	5	5	5	6
T_{SU} (ns)	3.7	3.7	3.7	4.0
T_{CO} (ns)	3.5	3.5	3.5	3.8
f_{SYSTEM} (MHz)	178	178	178	208

CPLD Xilinx – CoolRunner





CPLD from Lattice

The Do-it-All PLD - MachXO2
Offers an unprecedented mix of low cost, low power and high system integration for system and consumer designs

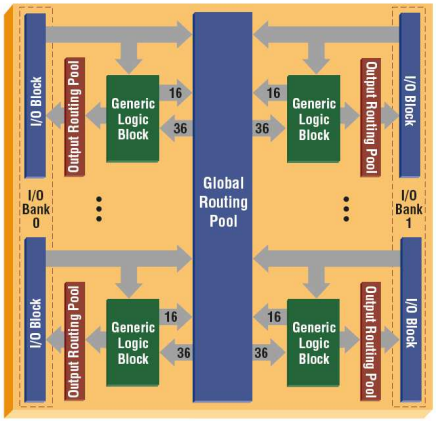
Most Versatile Non-Volatile PLD - MachXO
Combines FPGA flexibility with CPLD performance, instant-on and high pin to logic ratio

ispLEVER CLASSIC

Ultra Low Power CPLD - ispMACH 4000ZE
As low as 10µA standby current, packages as small as 4x4 mm, 5V-tolerant I/Os
+ Mature devices
(PAL, PALCE, GAL, ispGDX, ispLSI 1k..8k,ORCA,MACH 1,2,4)

Lattice ispMach4000 CPLD

ispMACH 4000 Block Diagram

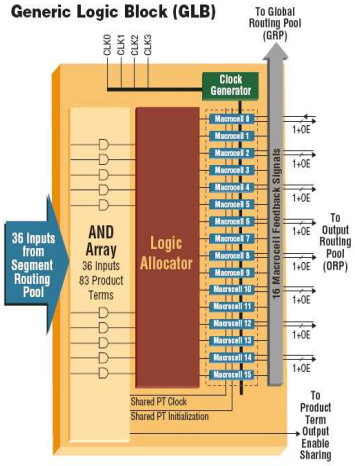


- SuperFAST Performance
  - 2.5 ns tPD Pin-to-Pin Delay
  - 400 MHz System Performance
- Industry's Lowest Power Consumption
  - 1.8V Core for Low Dynamic Power
  - Low Static Current
  - 1.3-3 mA (1.8V Device Family)
  - 11.3-13 mA (2.5V and 3.3V Device Families)
- Multiple Temperature Range Options
  - Commercial: 0 to 70º C TA (Ambient)
  - Industrial: -40 to 85ş C TA (Ambient)
  - Automotive: -40 to 125ş C TA (Ambient)
- Ease of Design
  - Excellent First-Time Fit and Refit Capability
  - 4 Global Clocks
  - 36 Inputs per Logic Block
  - Up to 80 Product Terms (PT) per Output
  - ORP for Pin Locking
  - Density Migration
  - Flexible Control, Clocking and OE
  - Fast, SpeedLocking™, and Wide PT Paths
  - 5V Tolerant Inputs and I/O
- Easy System Integration
  - Operation with 1.8V, 2.5V and 3.3V Supplies
  - 1.8V, 2.5V, 3.3V I/O Support
  - IEEE 1532 In-System Programmable (ISP™)
  - IEEE 1149.1 Boundary Scan Test
  - Open Drain Output for Flexible Bus Interface Capability
  - Programmable Pull-Up or Bus-Keeper Inputs
  - Hot Socketing Capability
  - 3.3V PCI Compatible
  - Programmable Output Slew Rate
  - Lead-free Package Options

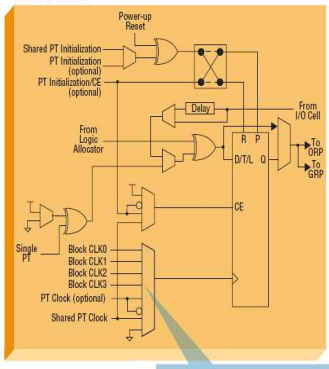
Lattice ispMach4000 CPLD

ispMACH 4000 Architecture

Generic Logic Block (GLB)



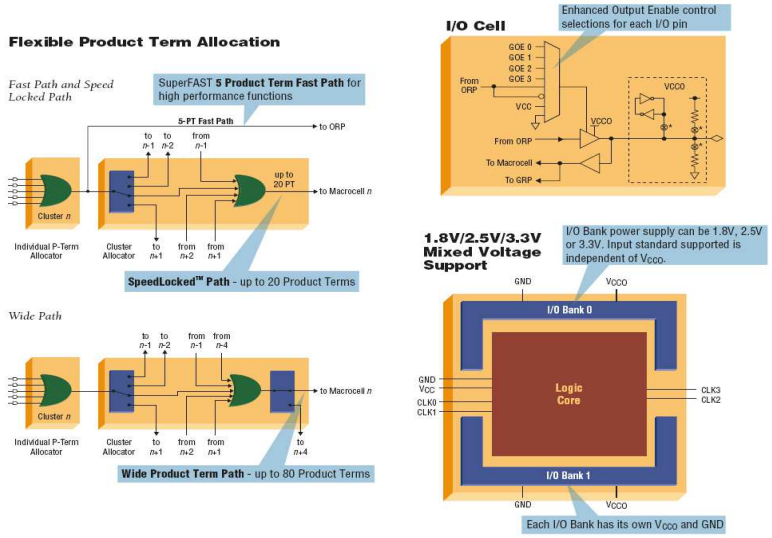
Macrocell



Flexible and efficient clock and control scheme ensures easy implementation with a variety of HDL coding styles.

J.Kasperek & P.J.Rajda © 2017 Katedra Elektroniki AGH

Lattice ispMach4000 CPLD



Altera CPLD

MAX V
- Robust features at up to 50 percent lower total power vs. competitive CPLDs
- Lower total system cost through architecture that integrates previously external functions
- Instant-on, single-chip CPLD built on non-volatile architecture

MAX II
- Instant-on, non-volatile, single-chip CPLD solution
- 1/10th the power of MAX CPLDs, with low cost, low power and high density
- On-board user flash memory. 1.8-V, 2.5-V, and 3.3-V supply voltages

MAX
- Instant-on, non-volatile, lov
- Deterministic timing
- 5.0-V I/O support. 2.5-V, 3

Układy
MAX V, MAX II, MAX

Software – Quartus II
(free for CPLD ...)

CPLD Altera – series MAX V

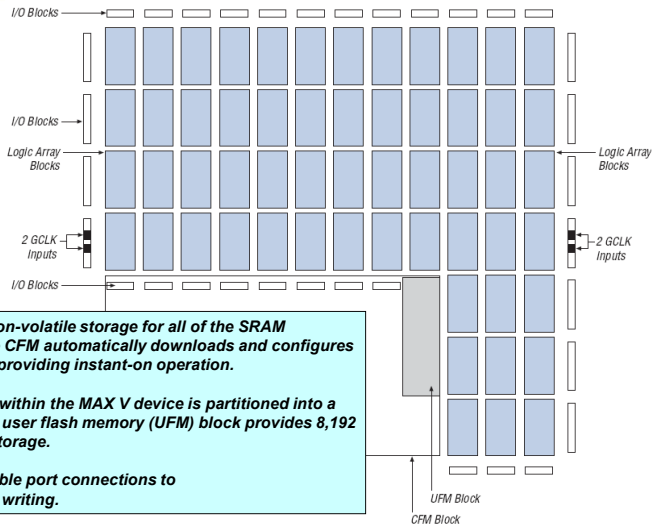
Feature Summary *The following list summarizes the MAX V device family features:*

Low-cost, low-power, and non-volatile CPLD architecture
Instant-on (0.5 ms or less) configuration time
Standby current as low as 25 µA and fast power-down/reset operation
Fast propagation delay and clock-to-output times
Internal oscillator
Emulated RSDS output support with a data rate of up to 200 Mbps
Emulated LVDS output support with a data rate of up to 304 Mbps
Four global clocks with two clocks available per logic array block (LAB)
User flash memory block up to 8 Kbits for non-volatile storage with up to 1000 read/write cycles
Single 1.8-V external supply for device core
MultiVolt I/O interface supporting 3.3-V, 2.5-V, 1.8-V, 1.5-V, and 1.2-V logic levels
Bus-friendly architecture including programmable slew rate, drive strength, bus-hold, andprogrammable pull-up resistor
Schmitt triggers enabling nois tolerant inputs (programmable per pin)

Table 1–1. MAX V Family Features

Feature	5M40Z	5M80Z	5M160Z	5M240Z	5M570Z	5M1270Z	5M2210Z
LEs	40	80	160	240	570	1,270	2,210
Typical Equivalent Macrocells	32	64	128	192	440	980	1,700
User Flash Memory Size (bits)	8,192	8,192	8,192	8,192	8,192	8,192	8,192
Global Clocks	4	4	4	4	4	4	4
Internal Oscillator	1	1	1	1	1	1	1
Maximum User I/O pins	54	79	79	114	159	271	271

CPLD Altera MAX V - architecture

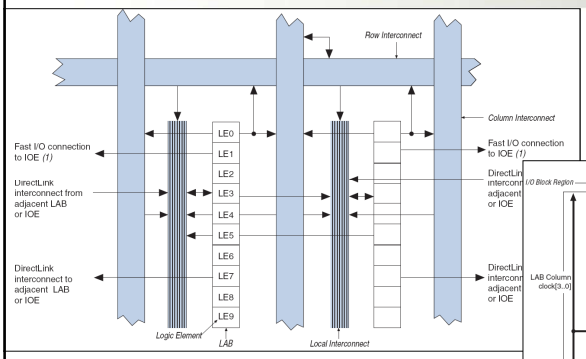


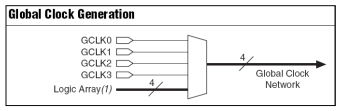
The CFM block provides the non-volatile storage for all of the SRAM configuration information. The CFM automatically downloads and configures the logic and I/O at power-up, providing instant-on operation.

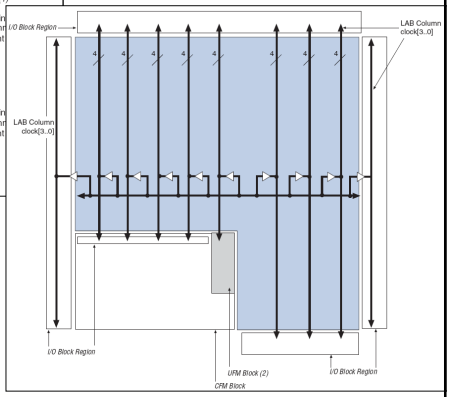
A portion of the flash memory within the MAX V device is partitioned into a small block for user data. This user flash memory (UFM) block provides 8,192 bits of general-purpose user storage.

The UFM provides programmable port connections to the logic array for reading and writing.

CPLD Altera MAX V - connections

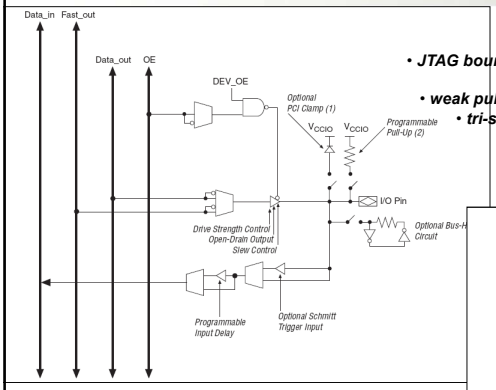






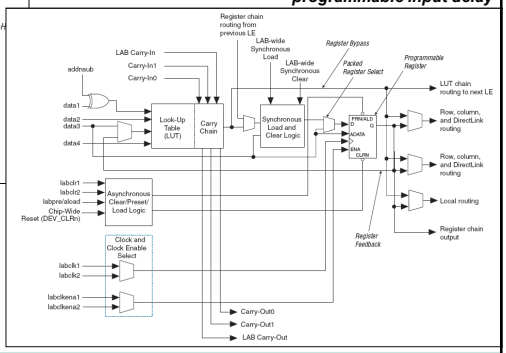
- LE grouped in 10 at *Logic Array Block*
- Connection buses – rows, columns
- Direct connections to LAB
- Direct connections to I/O
- Global clk networks

CPLD Altera MAX V –I/O blocks and LE



I/O block

- ***LVTTL, LVCMOS, LVDS, and RSDS I/O standards***
- ***JTAG boundary-scan test (BST) support programmable drive strength control***
- ***weak pull-up resistors during power-up and in system programming***
- ***tri-state buffers with individual output enable bus-hold circuitry***
- ***programmable pull-up resistors in user mode***
- ***open-drain outputs***
- ***Schmitt trigger inputs,***
- ***programmable input delay***



Each LE contains:

- ***four-input LUT,***
- ***programmable register (D, T, JK, or SR operation)***
- ***carry chain with carry-select capability.***
- ***supports dynamic single-bit addition or subtraction mode***
- ***clock enable, preset, asynchronous load, and asynchronous data.***

CPLD applications – Lattice marketing data

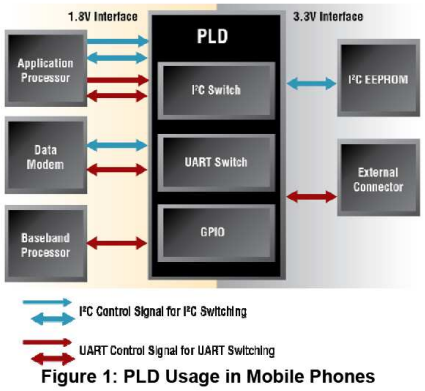


Figure 1: PLD Usage in Mobile Phones

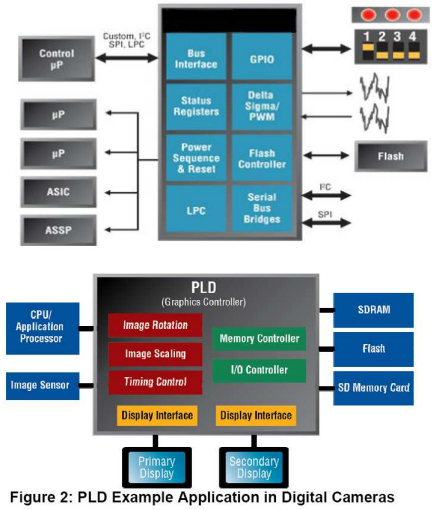


Figure 2: PLD Example Application in Digital Cameras

CPLD applications – Xilinx marketing data

Xilinx CPLD Applications Handbook

Featuring CoolRunner-II and XC9500XL CPLDs

CoolRunner-II XILINX®

This Chapter contains the following topics:

- *IrDA and UART Design in a CoolRunner CPLD*
- *Serial ADC Interface Using a CoolRunner CPLD*
- *Wireless Transceiver for the CoolRunner CPLD*
- *CoolRunner-II Smart Card Reader*
- *CoolRunner-II CPLD I2C Bus Controller Implementation*
- *CoolRunner-II Serial Peripheral Interface Master*
- *Design of a Digital Camera with CoolRunner-II CPLDs*
- *CompactFlash Card Interface for CoolRunner-II CPLDs*
- *Interfacing to Mobile SDRAM with CoolRunner-II CPLDs*
- *An SMBus/I2C-Compatible Port Expander*
- *Driving LEDs with Xilinx CPLDs*
- *CoolRunner-II CPLDs in Cell Phone Handsets/Terminals*
- *Implementing Keypad Scanners with CoolRunner-II*
- *Level Translation Using Xilinx CoolRunner-II CPLDs*
- *CoolRunner-II Character LCD Module Interface*
- *Using Xilinx CPLDs to Interface to a NAND Flash Memory Device*
- *Cell Phone Security Demoboard On The Fly Reconfiguration Technique*
- *Using CoolRunner-II with OMAP, XScale, i.MX & Other Chipsets*
- *Connecting Intel PXA27x Processors to Hard-Disk Drives with a CoolRunner-II CPLD*
- *A Low-Power IDE Controller Design Using a CoolRunner-II CPLD*
- *Using a Xilinx CoolRunner-II CPLD as a Data Stream Switch*
- *Supporting Multiple SD Devices with CoolRunner-II CPLDs*

CPLD applications – Altera marketing data