FPGA architectures Part 1

Agenda

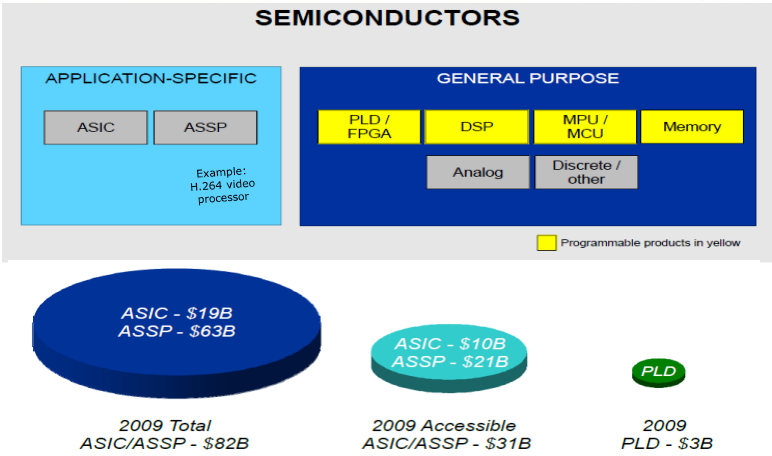
- ASIC vs ASSP vs FPGA
- FPGA devices
  - Features
  - Market data
- FPGA architecture
- Xilinx FPGA
  - Spartan 3
  - Spartan 6 Virtex 6
  - 7 Series
  - EasyPath

References

WWW FPGA manufactures

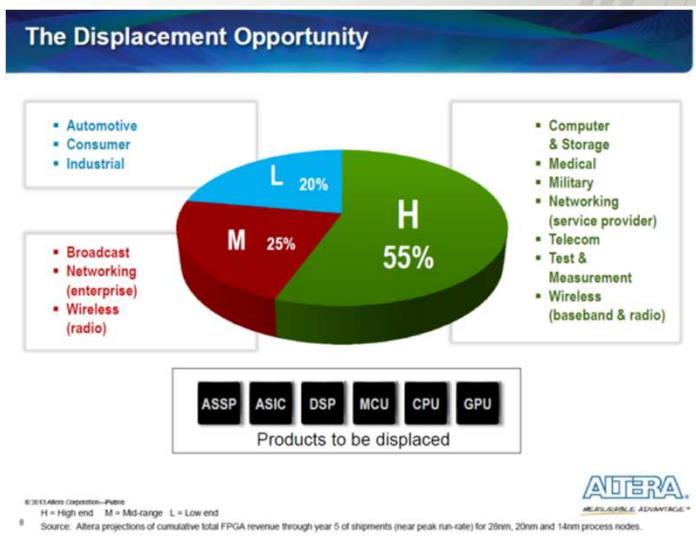
- Big labels (in alphabetical order)
  - www.actel.com (Microsemi)
  - www.altera.com (Intel)
  - www.atmel.com (Microchip)
  - www.latticesemi.com
  - www.quicklogic.com
  - **www.xilinx.com (this lecture)** (alliance with IBM since Nov 16, 2015)
- FPGA startups
  - http://www.achronix.com embedded FPGA (eFPGA)
  - http://www.siliconbluetech.com – acquired by LatticeSemiconductor
  - http://www.tabula.com ⊗ Feb 2015 closed
- extras
  - http://www.easic.com
- general
  - www.eetimes.com/design/programmable-logic-designline

ASIC? ASSP? or FPGA?

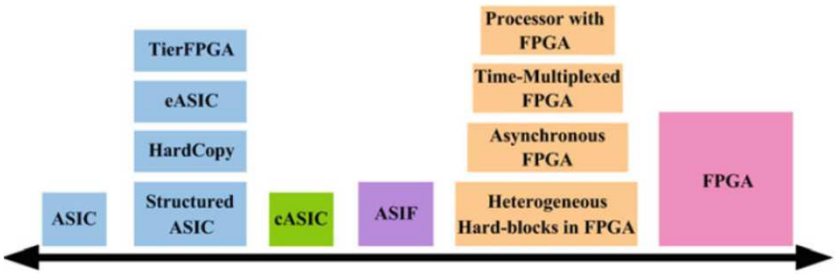


Capturing 1% of the Accessible ASIC/ASSP Market Drives 10% growth for the PLD Market

ASIC? ASSP? or FPGA?



ASIC ⇔ FPGA

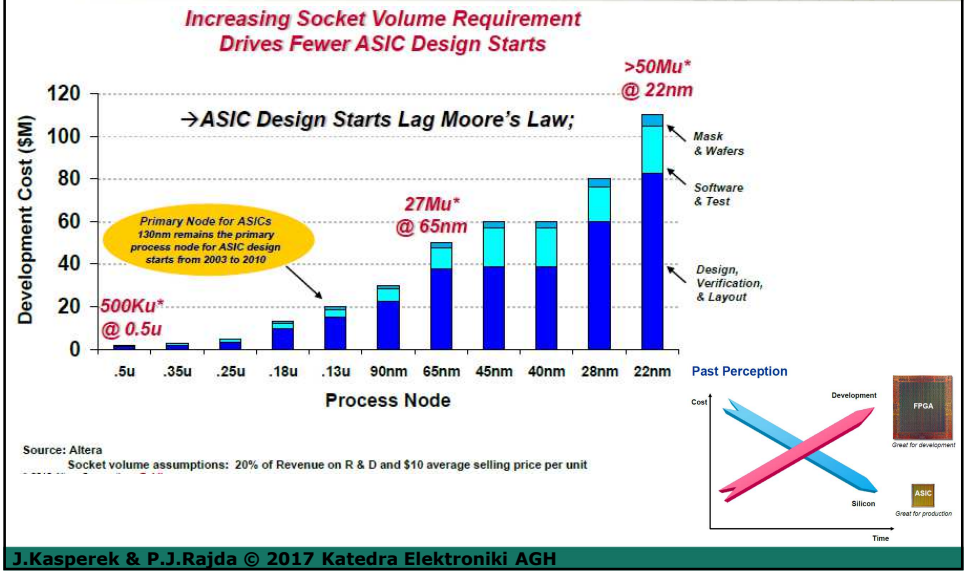


+ High Performance
+ High Volumn Production
+ Low Area
+ Low Power Consumption
– Low Reusability
– Low Flexibility
– High NRE
– High Time-to-market

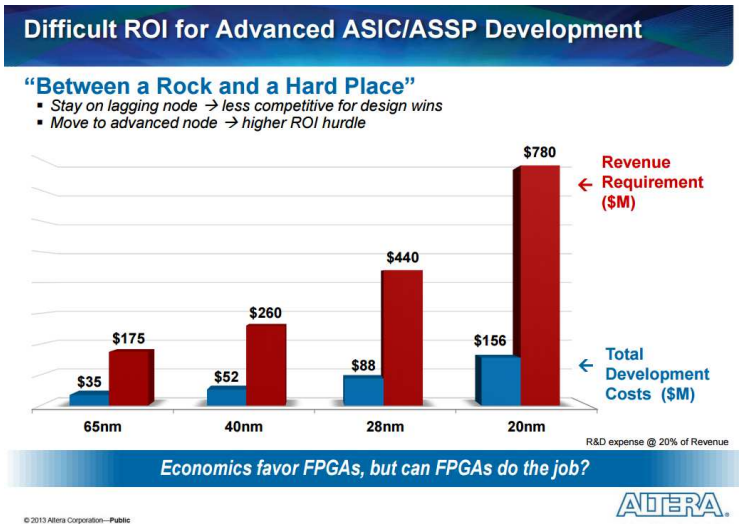
High Flexibility +
High Reusability +
Low Time-to-market +
Low NRE +
High Area –
Low Performance –
High Power Consumption –
Low Volume Production –

Non-recurring engineering (NRE) refers to the one-time cost to research, develop, design and test a new product.

ASIC? ASSP? or FPGA?

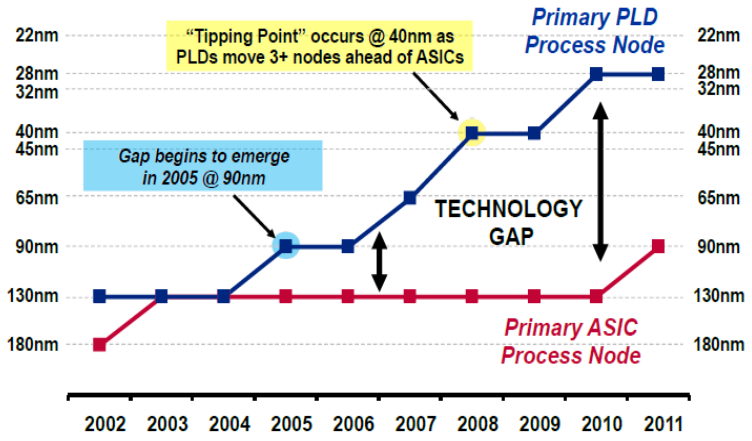


ASIC? ASSP? or FPGA?



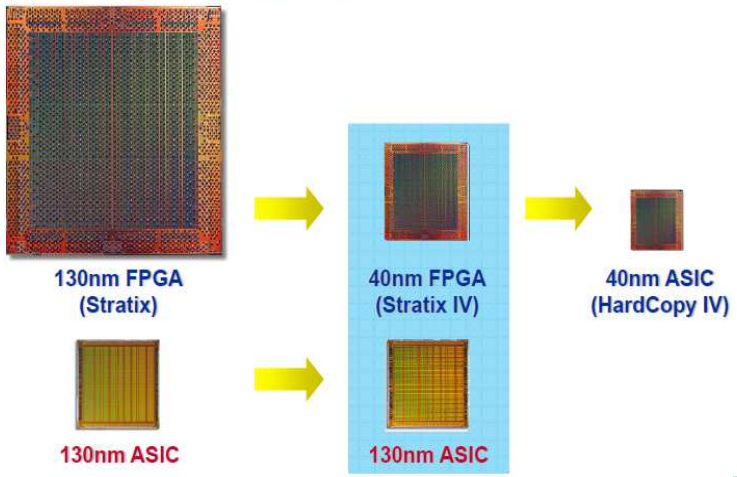
ASIC? ASSP? or FPGA?

PLD v ASIC "Tipping Point"



ASIC? ASSP? or FPGA?

Reaching the Tipping Point



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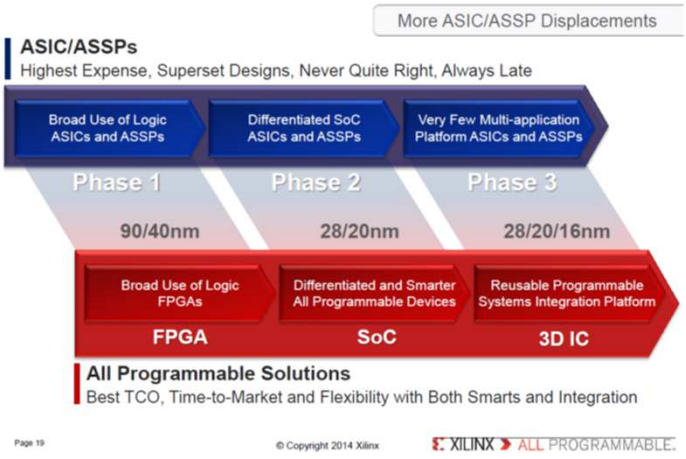
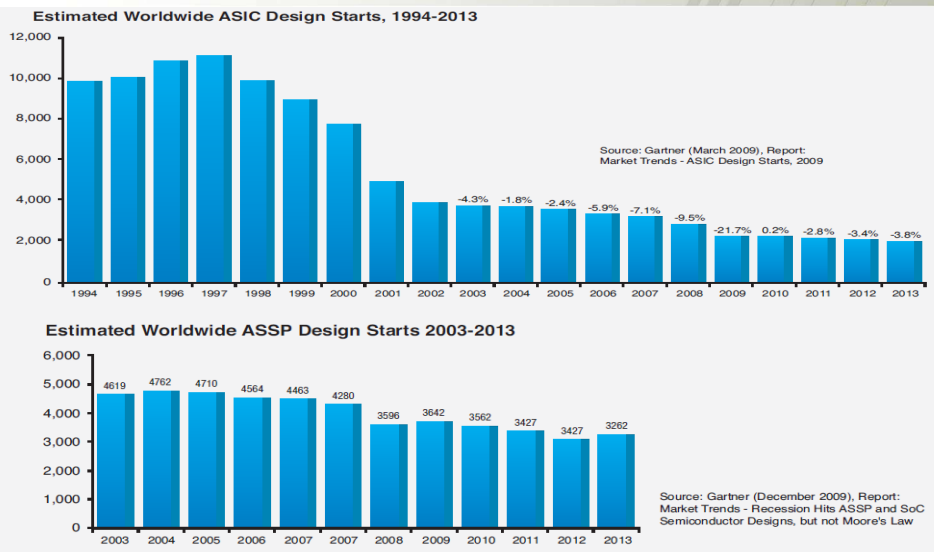
ASIC? ASSP? or FPGA?

Accelerating Growth From ASIC/ASSP Evolution



ASIC? ASSP? or FPGA?



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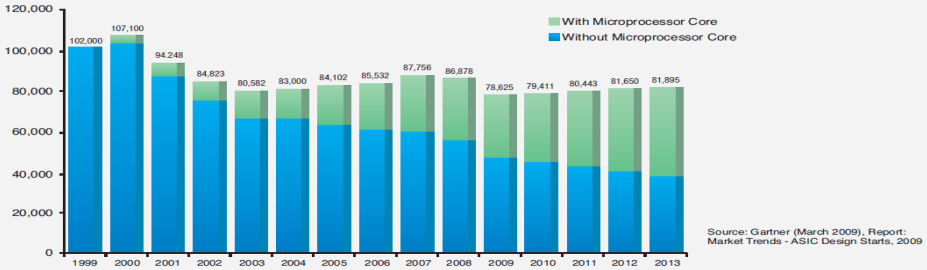
ASIC? ASSP? or FPGA?

Estimated FPGA /PLD Design Starts, 2003-2013



Source: Gartner (March 2009), Report: Market Trends - ASIC Design Starts, 2009

Application	Product Displaced
Security Access Control	ASSP
Security Surveillance	ASSP
Print-Head Interface	ASIC
GPS Anti-Jammer	ASIC
STS12 Framer/Mapper	ASIC
40G Transponder	ASSP
40G Muxponder	ASSP
Image Processing	ASSP
Rear View Camera	ASSP
Instrument Cluster Display	ASSP
Graphics Display Controller	ASSP
1394 Interface	ASSP
Image Processing	ASSP
Video Controller	ASSP
Wireless Radio	ASSP

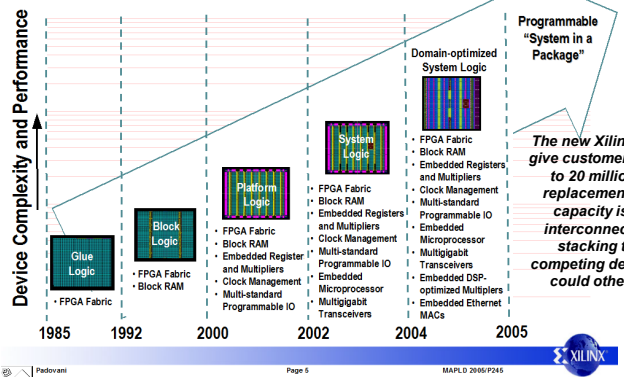
Application	Product Displaced
Multi Viewer Equipment	ASSP
OC768 Framer	ASSP
DDC and DUC	ASSP
Framers and FECs	ASIC
Cryptography Equipment	ASIC
Storage Crypto	ASIC
40/100G Ethernet Tester	ASSP
Flash Interface for SSD	ASIC
40/100G Ethernet Tester	ASSP
Enterprise Switching – 4 x 40GE LC	ASIC
Edge Router – Core Space/Data Center	ASIC
eQAM	ASSP
CMTS Router	ASSP
Next Gen Switch	ASIC
Security/Firewall	ASSP

Application	Product Displaced
Security Encryption	ASSP
Security Coprocessing	ASIC
100G Muxponder	ASSP
GPON – Traffic Management	ASSP
Switch Fabric	ASIC
Video Switch	ASIC
Print Engine	ASIC
Beam Forming	ASIC
DDC/DUC	ASSP
Custom Southbridge Companion Chip	ASIC
Traffic Manager	ASIC
OC-3/OC-12 Clock Data Recovery	ASSP
1588 Slave Clock Function	ASIC

Xilinx: FPGA inventor story

Our first FPGA, the XC2064, was shipped in 1985; it offered 800 gates, sold for $55, and was produced on a 2.0µ process. We have been shipping that device for 15 years and today it sells for just $5.
by Wim Roelandts, CEO, Xilinx (1999 Xcell 32)

Architectural Evolution
Reconfigurable FPGAs



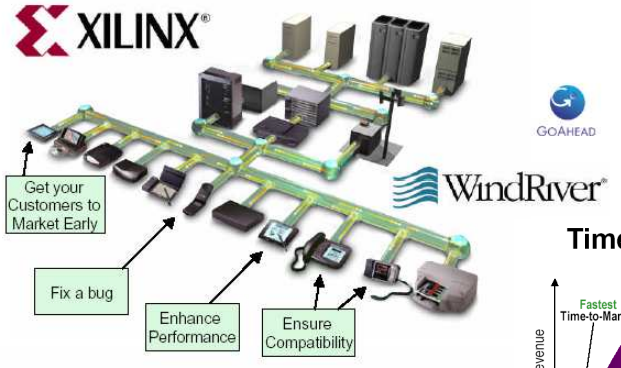
The new Xilinx FPGA is built using 6.8 billion transistors to give customers access to two million logic cells, equivalent to 20 million ASIC gates, for system integration, ASIC replacement, and ASIC prototyping and emulation. This capacity is made possible by Xilinx's stacked silicon interconnect technology, the first application of 2.5D IC stacking that gives customers twice the capacity of competing devices and leaping ahead of what Moore's Law could otherwise offer in a monolithic 28nm FPGA, the company said.

FPGA features

- **Perfect technology for embedded systems market**
  Fast Time-to-Market
- **Integration benefits**
  lower costs, lower power consumption, small size, System on Chip
- **Lower costs and lower risks then ASIC,**
  no NRE (Non-Recurring Engineering)
  minimum order size nor inventory risk,
  no long delay in design and testing
- **Extreme high data processind speed**
  massively parallel operation much faster than DSP engines
- **Programmable at every stage of development and usage**
  in design, in manufacturing, after installation
  allows unlimited product differentiation

Internet Recofigurable Logic

Remote update of software and hardware

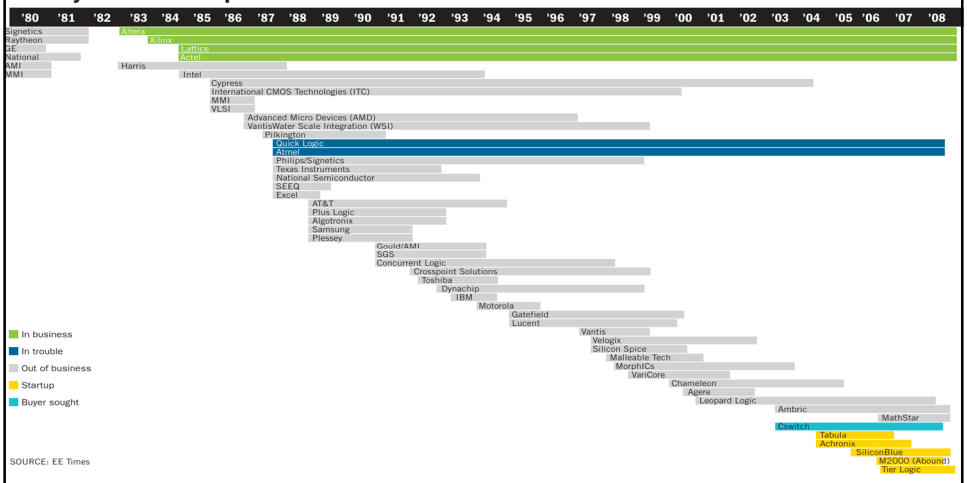


Time-to-Market Value

Quicker time-to-market and reprogrammability provide the best chance of achieving full product profit potential

PLD companies

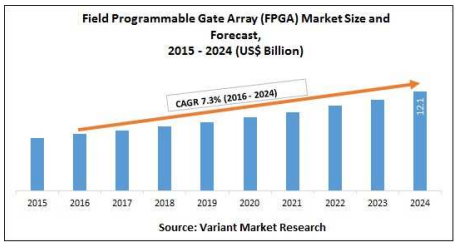
History of PLD startups



FPGA market data

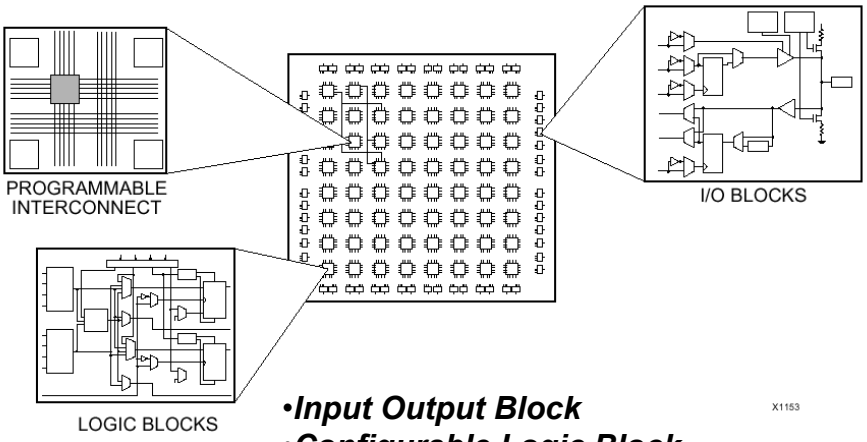
Vendor	2015 FPGA Total	2015 Market share	2016 FPGA Total	2016 Market share	Growth CY15-CY16
Xilinx	$2,044	53%	$2,167	53%	6%
Intel (Altera)	$1,389	36%	$1,486	36%	7%
Microsemi	$301	8%	$297	7%	-1%
Lattice	$124	3%	$144	3%	16%
QuickLogic	$19	0%	$11	0%	-40%
Others	$2	0%	$2	0%	0%
TOTAL	$3,879	100%	$4,112	100%	6%

https://www.eetimes.com/author.asp?doc_id=1331443



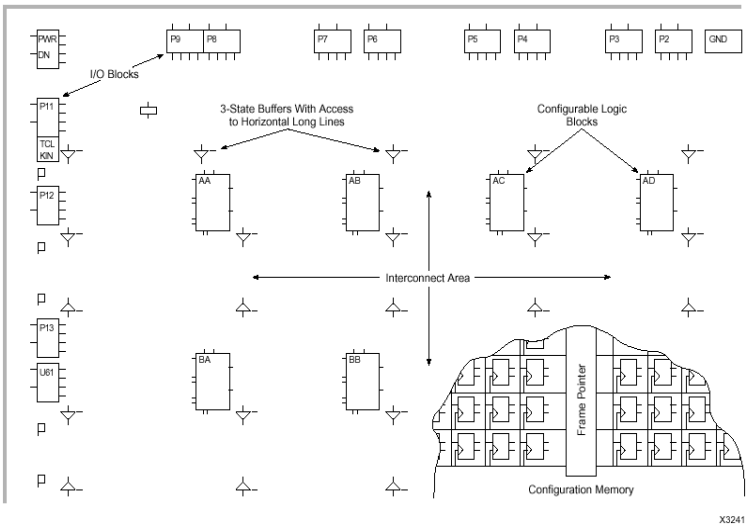
https://www.variantmarketresearch.com/report-categories/semiconductor-electronics/field-programmable-gate-array-market

General FPGA architecture

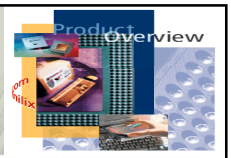


- ***Input Output Block***
- ***Configurable Logic Block***
- ***Connections & routing resources***

General FPGA architecture



FPGA XILINX story



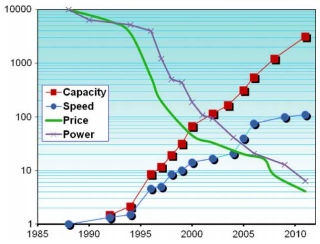


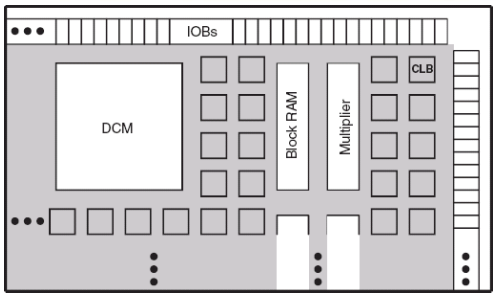
Fig. 1. *Xilinx FPGA attributes relative to 1988. Capacity is logic cell count. Speed is same-function performance in programmable fabric. Price is per logic cell. Power is per logic cell. Price and power are scaled up by 10 000×. Data: Xilinx published data.*

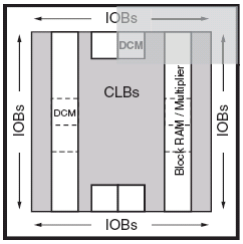
- **XC 2000**
  1985 0,8...1,5 tys. LGEs
- **XC 3000 & 3100 /A/L**
  1987 1,5...7,5 tys. LGEs
- **XC 4000 : A/H/D/E/L/EX/XL/XLT/XLA/XV**
  1990 2...250tys. LGEs
- **XC 5200**
  1994 3...23 tys. LGEs
- **XC 6200**
  1996 13...100 tys. LGEs

- **XCS /XL (Spartan)**
  1997 5...40 tys. LGEs
- **XCV – E/EM (Virtex)**
  1998 58... 4.074 tys. LGEs
- **XCS-2 (Spartan-2)**
  2000 15...200 tys. LGEs
- **XCV-2 (Virtex-2)**
  2001 40...10.000 tys. LGEs
- **XCS-3 (Spartan-3)**
  2004
- **XCV-4 (Virtex-4)**
  2004
- **XCV-5 (Virtex-5)**
  2007
- **XCS-6 (Spartan-6)**
  2009 3,8...147 tys. Logic Cells
- **XCV-6 (Virtex-6)**
  2009 75...567 tys. Logic Cells
- **XCV-7 (Virtex-7,Artix-7,Kintex-7)**
  2010-2011 8...1955 tys. Logic Cells

Now they are selling 28nm
aiming at 16…20 nm devices with IBM

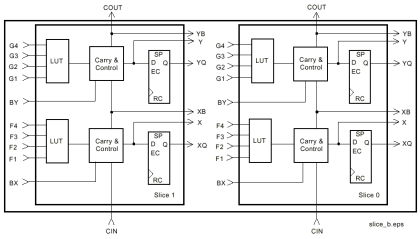
Xilinx Spartan3

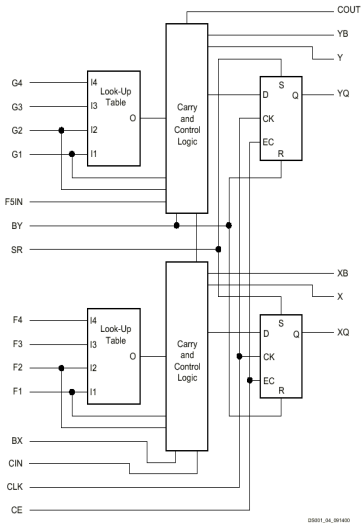




- technology 90nm
- coarse grain structure
- 50k – 5.000k system gates
- 725 MHz max toggle frequency
- clock – DCMs: 2...4
- 18-bits multipliers: 4...104
- memory Select RAM+
  - distributed: do 520 Kb
  - block (18Kb): do 1872 Kb
  - external
- SRAM configuration memory
  (4 modes + ReadBack)
- port JTAG
  (test + configuration)
- supply:
  - V_{CCINT} : 1,2V
  - V_{CCAUX} : 2,5V
  - V_{CCO} : 1,2...3,3V

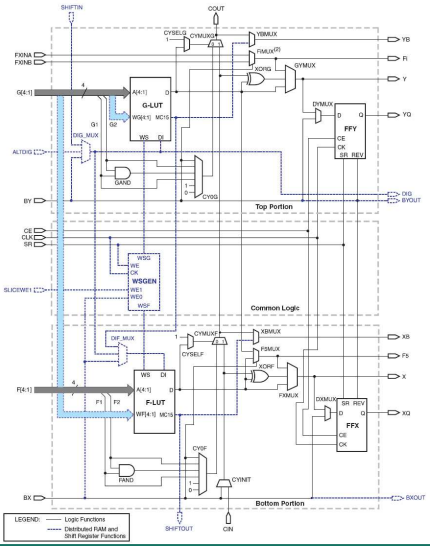
Xilinx Spartan3

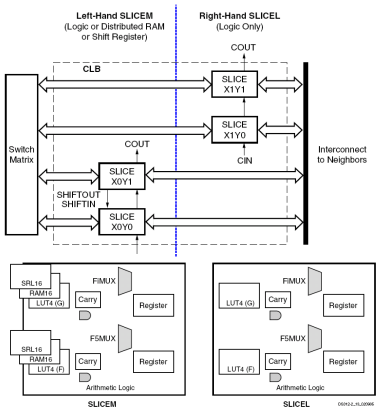




- **CLB = 2 x LS = 4 x LC**
  - **flip flop / latch**
  - ***Clock Enable***
  - **AP / AC / SS / SR**
  - **LUT (*Look-Up-Table*)**
  - ***carry logic***

Spartan3 CLB – LUT

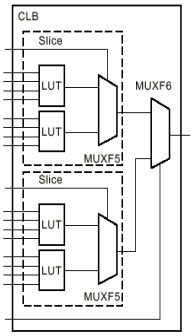


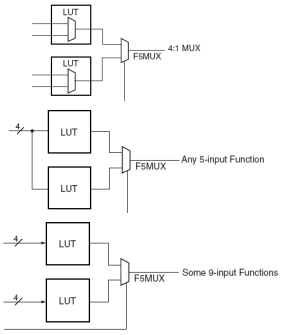


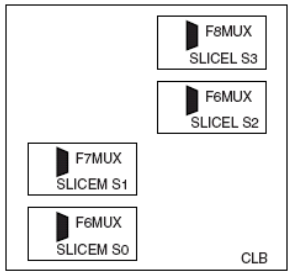
LUT:

- **4-inputs function generator**
- **SinglePort / DualPort RAM**
- **16-stages shift register**

Spartan3 CLB – multipleksery



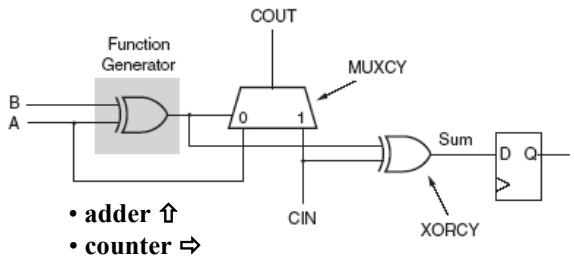




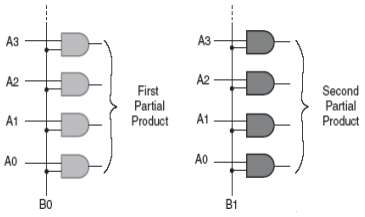
Mux	Usage	Input Source	Total Number of Inputs per Function		
			For Any Function	For Mux	For Limited Functions
F5MUX	F5MUX	LUTs	5	6 (4:1 mux)	9
FiMUX	F6MUX	F5MUX	6	11 (8:1 mux)	19
	F7MUX	F6MUX	7	20 (16:1 mux)	39
	F8MUX	F7MUX	8	37 (32:1 mux)	79

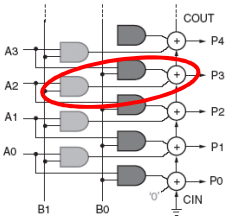
- no BUFT/BUFE
- bus function as mux
- other mux:
  CYMUX, BUFGMUX

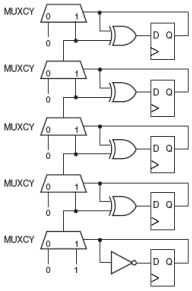
Spartan3 – Carry & Arithmetic logic

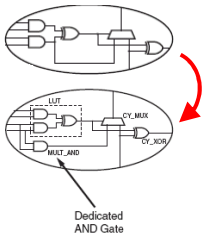


- adder ⇧
- counter ⇨
- multiplier ⇩

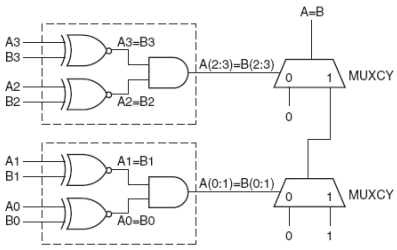


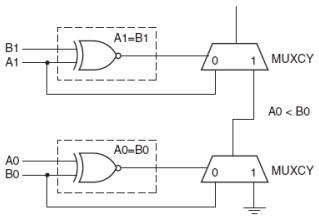


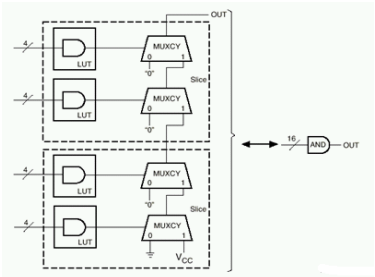




Spartan3 – Carry & Arithmetic logic

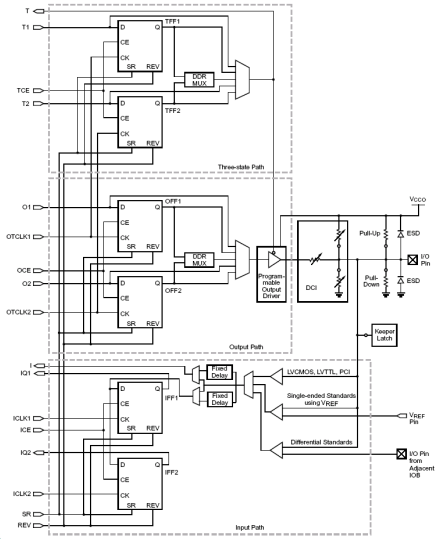






- *Equality Comparator* ⇧
- *Magnitude Comparator* ⇗
- *Wide-AND* ⇨

Spartan3 - IOB

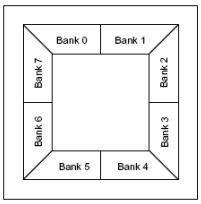


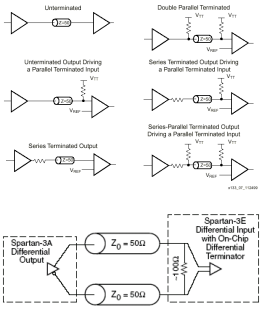
DDR:
- **flip flops pair**
- **DDR mux**
- **each core signal can be inverted**

Programmable:
- ***pull-up***
- ***pull-down***
- ***weak-keeper*** 🤞
- ***DCI*** *Digital Controlled Impedance*
- ***delay***

Spartan3 - IOB

5V interface possible with LVTTL buffers:
- **input (IBUF) – I_{IK} <100mA, <100 inputs**
- **output (OBUF, OBUFT) – optional *driver***
- **I/O (IOBUF) –**
- **clock. (IBUFG) –divider required**

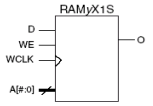


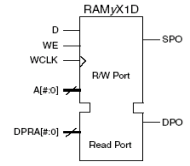


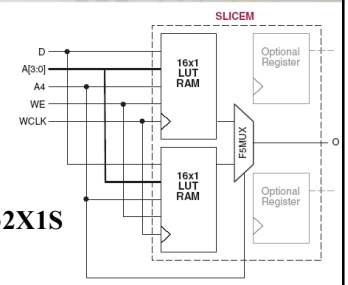
Standard Category	Description	V_{CCO} (V)	Class	Symbol (IOSTANDARD)	DCI Option
Single-Ended					
GTL	Gunning Transceiver Logic	N/A	Terminated	GTL	Yes
			Plus	GTLP	Yes
HSTL	High-Speed Transceiver Logic	1.5	I	HSTL_I	Yes
			III	HSTL_III	Yes
		1.8	I	HSTL_I_18	Yes
			II	HSTL_II_18	Yes
			III	HSTL_III_18	Yes
LVCMOS	Low-Voltage CMOS	1.2	N/A	LVCMOS12	No
		1.5	N/A	LVCMOS15	Yes
		1.8	N/A	LVCMOS18	Yes
		2.5	N/A	LVCMOS25	Yes
		3.3	N/A	LVCMOS33	Yes
LVTTL	Low-Voltage Transistor-Transistor Logic	3.3	N/A	LVTTL	No
PCI	Peripheral Component Interconnect	3.0	33 MHz(1)	PCI33_3	No
SSTL	Stub Series Terminated Logic	1.8	N/A (±6.7 mA)	SSTL18_I	Yes
			N/A (±13.4 mA)	SSTL18_II	No
		2.5	I	SSTL2_I	Yes
			II	SSTL2_II	Yes
Differential					
LDT (ULVDS)	Lightning Data Transport (HyperTransport™) Logic	2.5	N/A	LDT_25	No
LVDS	Low-Voltage Differential Signaling		Standard	LVDS_25	Yes
			Bus	BLVDS_25	No
			Extended Mode	LVDSEXT_25	Yes
LVPECL	Low-Voltage Positive Emitter-Coupled Logic	2.5	N/A	LVPECL_25	No
RSDS	Reduced-Swing Differential Signaling	2.5	N/A	RSDS_25	No
HSTL	Differential High-Speed Transceiver Logic	1.8	II	DIFF_HSTL_II_18	Yes
SSTL	Differential Stub Series Terminated Logic	2.5	II	DIFF_SSTL2_II	Yes

Spartan3 – LUT as Distributed RAM

Primitive	RAM Size (Depth x Width)	Type	Address Inputs
RAM16X1S	16 x 1	Single-port	A3, A2, A1, A0
RAM32X1S	32 x 1	Single-port	A4, A3, A2, A1, A0
RAM64X1S	64 x 1	Single-port	A5, A4, A3, A2, A1, A0
RAM16X1D	16 x 1	Dual-port	A3, A2, A1, A0

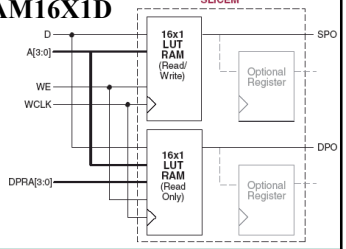






RAM32X1S

RAM16X1D

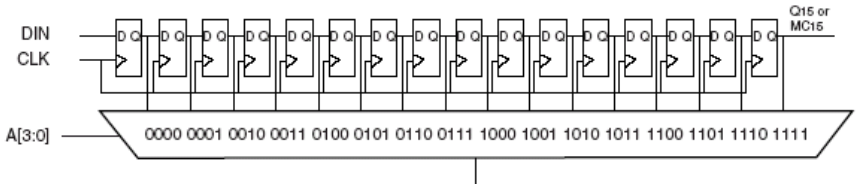


Element	Slices
RAM16X1D	1
RAM16X1D_1	1
RAM16X1S	0.5
RAM16X1S_1	0.5
RAM16X2S	1
RAM16X4S	2
RAM16X8S	4
RAM32X1S	1

Element	Slices
RAM32X1S_1	1
RAM32X2S	2
RAM32X4S	4
RAM32X8S	8
RAM64X1S	2
RAM64X1S_1	2
RAM64X2S	4
RAM128X1S	4

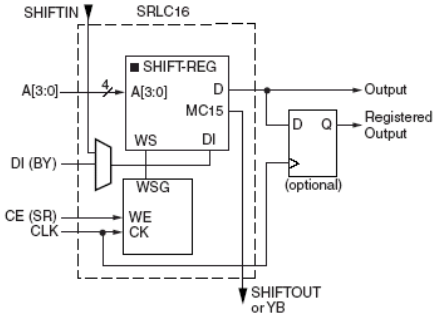
Element	Slices
RAM128X1S_1	4
ROM16X1	0.5
ROM32X1	1
ROM64X1	2
ROM128X1	4
ROM256X1	8

Spartan3 – LUT as Shift Register

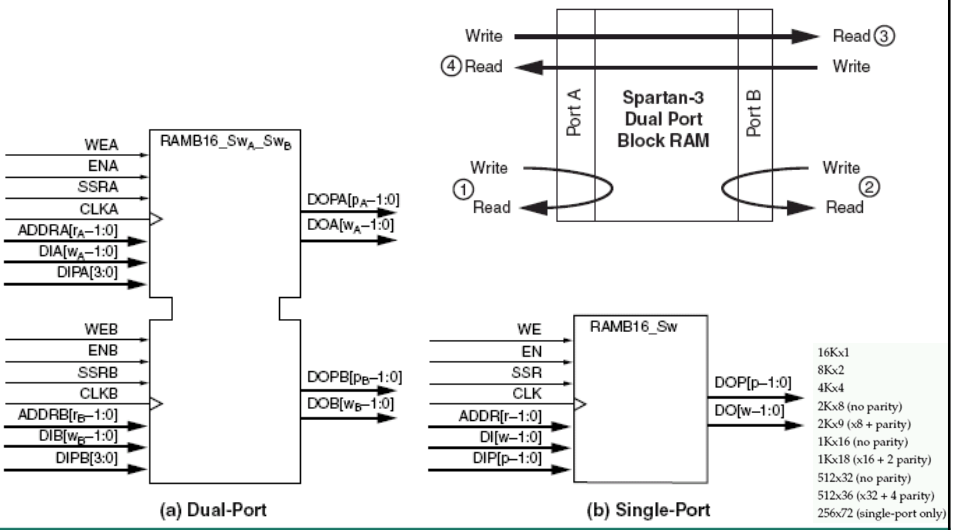


Applications:

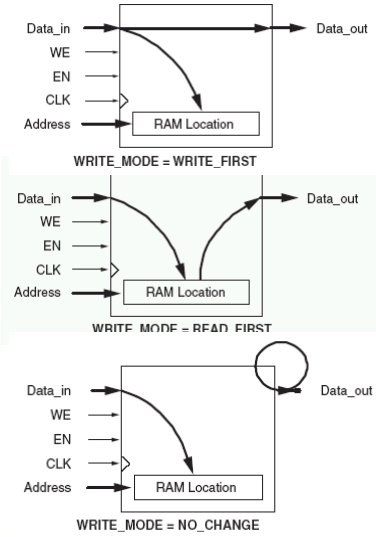
- long digital delay lines
- big capacity counters (also LFSR)
- synchronous FIFO
- pseudo random generators



Spartan3 – Block RAM



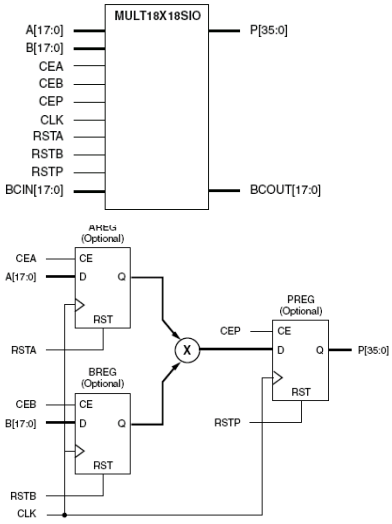
Spartan3 – Block RAM



Applications :

- big memories (cascading)
- ROM memories
- FIFO registers
- code memory for soft μP cores
- round buffers
- delay lines
- advanced FSM
- big logic functions
- fast big capacity counters
- CAM memories
- two port memories
- function tables (DDS)

Spartan3 – multipliers

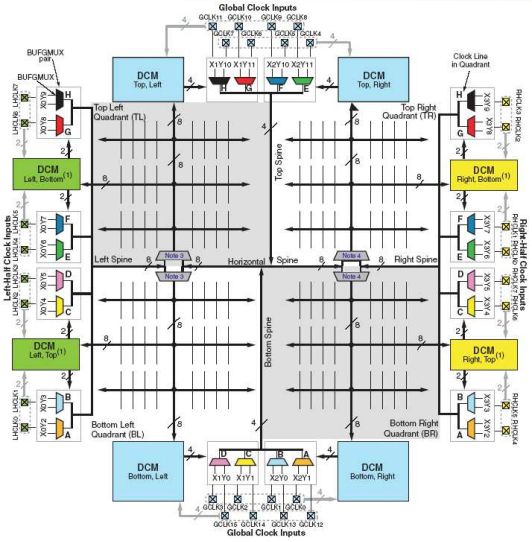


- 18-bits arguments
- 36-bits products
- U2 code
- optional registers

Applications:

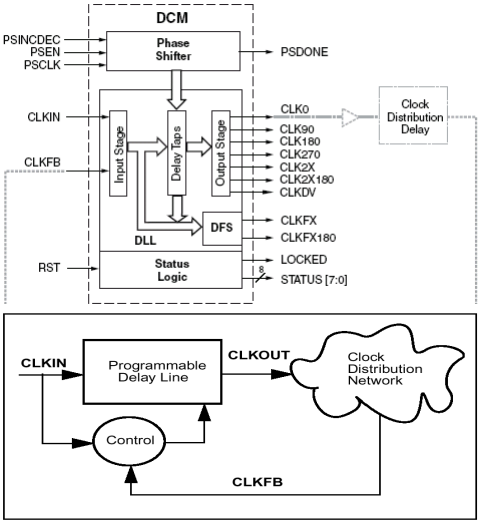
- multiplications
- shifting
- modulus
- U2 code actions
- complex number actions
- floating point

Spartan3 – Clock Resources



- 16 global clock inputs GCLK
- 8 inputs for local clock LH/RHCLK
- 2...8 DCM (*Digital Clock Manager*)
- „fractal like" distribution

Spartan3 – DCM



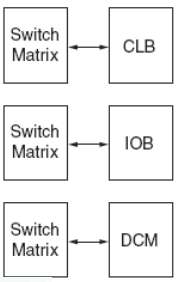
DCM blocks:
- **DLL** (Delay Locked Loop)
- **DFS** (Digital Frequency Synthesizer)
- **PS** (Phase Shifter)
- **Status Logic**

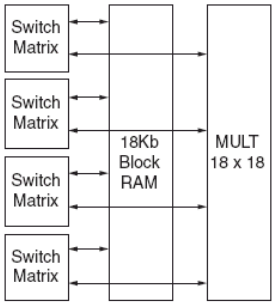
DCM functions :
- phase differencies elimination
- phase shifting
- clock multiplication / division
- duty ratio correction

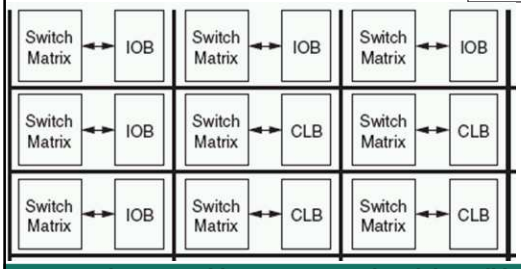
- DLL: $F_{in} \times 2$
- DLL: F_{in} / 1.5, 2, 2.5 ... 7.5, 8 ... 16
- DLL: F_{in} >> 0° / 90° / 180° / 270°
- DFS: $F_{in} \times M/D$; M=2...32, D=1..32

Spartan3 – interconnection resources

***Interconnect Tile*:**
Switch Matrix **connection**
(CLB, IOB, DCM, BRAM,MULT)







Connection resources:

- ***long lines***
- ***hex lines***
- ***double lines***
- ***direct lines***

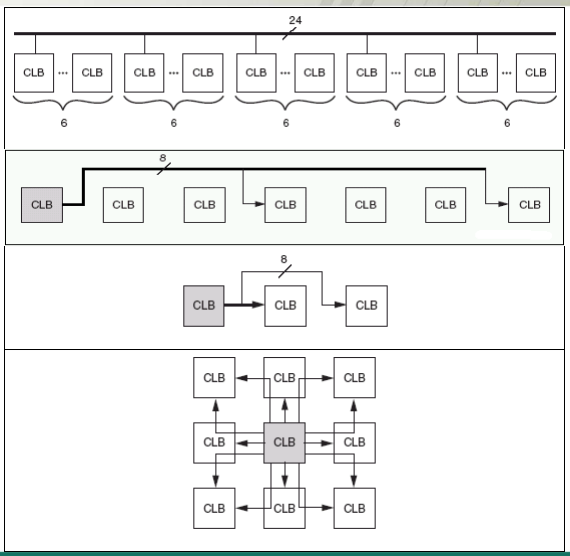
Spartan3 – interconnection resources

- **24 lines horizontal and vertical for every row and column spanned for the chip width**
- **every 6th Switch Matrix connection**

- **8 *hex* lines in 4 directions**
- **input at the start only**
- **output at the end and/or in the middle**
- **every 3rd Switch Matrix connection**

- **8 *double* lines in 4 directions**
- **input at the beggining only**
- **output at the end and/or in the middle**
- **every 3rd Switch Matrix connection**

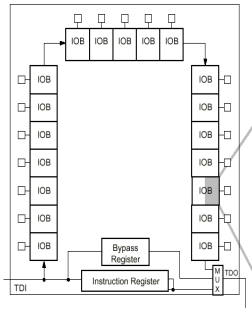
- ***direct*** **lines in 8 directions**

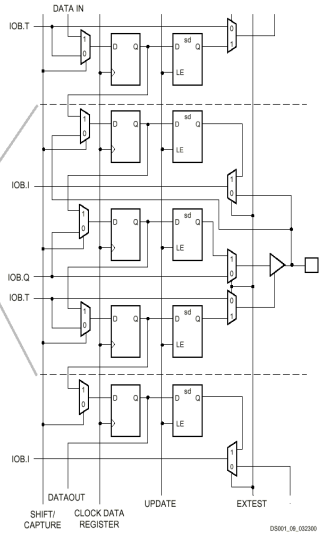


Spartan3 – configuration

Configuration modes :

- *Slave Serial*
- *Master Serial*
- *Slave Parallel (SelectMAP)*
- *Boundary Scan (JTAG)*





***ReadBack*:**

- **After programming verification**
- ***debug* read any flip flop**

Virtex6 Spartan6

Virtex-6 and Spartan-6 FPGA Families

- **Moore's Law**
  - Doubles the max capacity, compared to the previous generation
  - Reduces cost per function
- **Architecture and circuit innovations**
  - Increase speed and lower power consumption
- **Wide range of capacity, applications, cost**
  - Virtex-6 and Spartan-6 FPGAs cover a 250 : 1 capacity range
    - At the high end: Virtex-6 covers a 10 : 1 ratio
    - At the low end: Spartan-6 covers a 40 : 1 ratio
      - The name always indicates the logic capacity: XC6V760 to XC6S4
- **Virtex-6 and Spartan-6 share architecture, technology, software**
  - Different emphasis on cost, performance, power, size, packaging

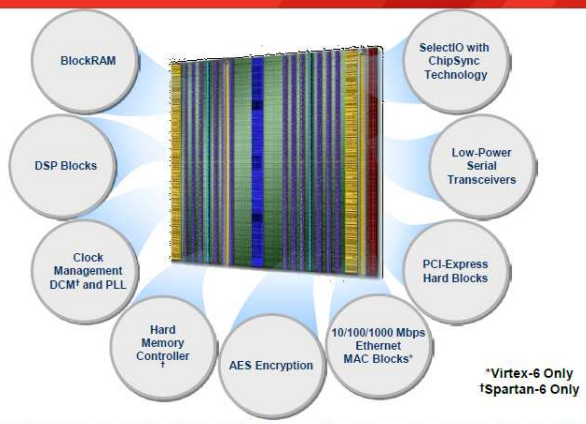
Virtex6 Spartan6

Spartan-6 and Virtex-6 Overview

	Spartan-6	Virtex-6
Logic Cells	4K → 150K	75K → 760K
LUT6	2.5K → 92K	47K → 474K
FF	5K → 184K	93K → 948K
BRAM (kbits)	216 Kb → 4.8 Mb	5.5 Mb → 38.3 Mb
DSP48	8 → 180	288 → 2016
DSP48 FMax	283 MHz	600MHz
Processing Performance	51 GMAC	1210 GMAC

Virtex6 Spartan6

Virtex-6 and Spartan-6 Hard-IP Blocks

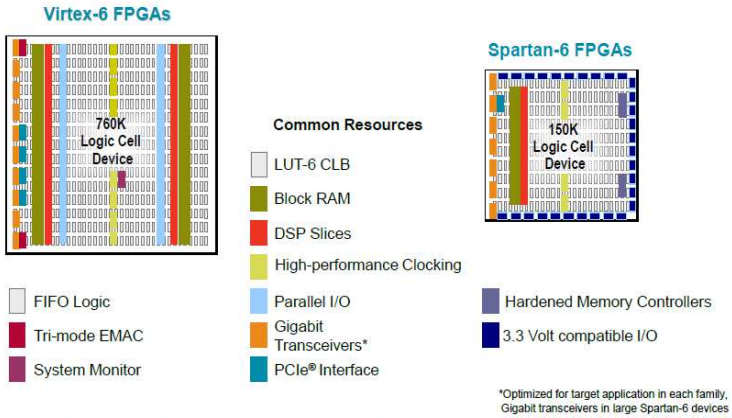


Hard IP blocks for widely-used functions: faster, more efficient, lower power
Careful choice: every user must pay for these functions, whether used or not

J.Kasperek & P.J.Rajda © 2017 Katedra Elektroniki AGH

Virtex6 Spartan6

Virtex-6 and Spartan-6 Architecture Alignment



Enables design portability, allows design re-use

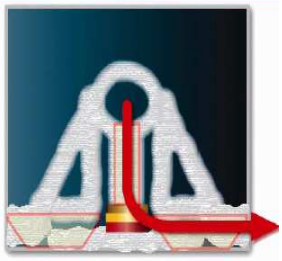
Virtex6

What is Virtex-6 ?

- **Next Generation 40nm Virtex Product Family**
  - Increase in size, density and cost reduction compared to Virtex-5
  - Increased speed and reduced power mainly through architecture and cicuitry
  - Evolutionary Feature Enhancements from Virtex-5
- **Three Platforms**
  - **LXT:** popular mix of logic, memory, DSP and serial connectivity
  - **SXT:** additional DSPand Memory, same serial connectivity
  - **HXT:** adds 11.2 Gbps transceivers for highest total bandwidth
- **Staged Rollout**
  - **LXT & SXT:** "ES" 3Q09, General avalability 4Q09, Production early 2010
  - **HXT:** Production 2010

Virtex6

Power Focus: Process and Circuit Innovation



- **Low static power (controlled leakage)**
  - 3rd generations of Triple Oxide innovation
    - Fast transistors wherever needed, low leakage everywhere else
  - Speed without additional leakage:
    - Silicon Germanium (SiGe) implant layer
    - Strained silicon
- **Low dynamic power**
  - Process shrink and low-K dielectric material
  - Vccint = 1.0 V with 0.9 V option
    - 20% lower power @ 10% lower speed

Virtex6

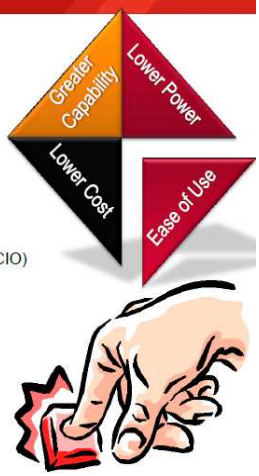
Performance Improvements, Virtex-6 over Virtex-5

- **Logic: 15% faster**
  - Advanced process, improved routing, faster pipelining
- **Serial Transceivers: 86% higher total bandwidth**
  - Up to 72 transceivers delivering 580 Gbps in Virtex-6 HXT
  - Compared to 48 transceivers delivering 312 Gbps in Virtex-5 TXT
- **General-purpose I/O: 33% higher bandwidth**
  - Enables advanced memory interfaces (DDR3)
- **Global clocking: 10% faster**
  - Lower skew, improved jitter, faster clock trees
- **DSP bandwidth more than doubled**
  - Over 2,000 enhanced DSP slices

Virtex6

Ease of Use and Lower Cost

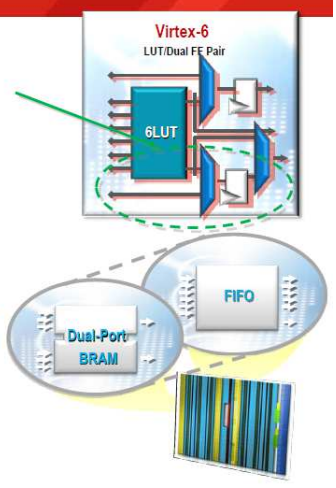
- **Designed to be backward compatible with Virtex-5**
  - Same GTX, SelectIO, BRAM, MMCM, & LUT6 primitives
  - Superset of CLB and DSP fratures
- **Simple IO planning and board layout**
  - All IOs support all standards at all speeds, period.
  - Homogenous IOs simplify layout
- **Simple power supply planning**
  - Requires only three power supplies. (VCCINT, VCCAUX & VCCIO)
  - Embedded decoupling capacitors
- **Shorter Time to Market**
  - Easy Migration from previous generations
  - Large set of available and portable IPs



Virtex6

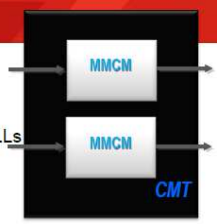
Virtex-6 Logic and BlockRAMs

- ***CLB differences from Virtex-5***
  - Double the number of flip-flops
  - Much more efficient pipelining
- ***Block RAMs same as in Virtex-5***
  - Higher memory / logic ratio in LXT
  - Up to 38 Megabits of Block RAM
  - Still the same features:
    - 36k Block splittable in 2x 18k Blocks
    - Single-port, simple dual-port and true dual-port
    - Read before write, as well as write before read
    - FIFO option
- ***Don't tamper with success***

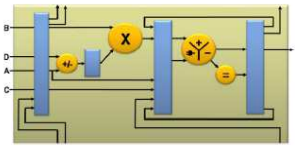


Virtex6

Clocking and DSP



- *Large chips + high speed pose challenges*
- *Multiple clocks derived on-chip*
  - Mixed Mode Clock Manager (MMCM) replaces DCMs and PLLs
    - PLL-based technology with DCM-like enhancements
- *Very large chips need large Global Clock trees*
  - High fan-out, low delay, low skew, low jitter
    - Fan-out is driven from the center
    - In spite of this, largest chip lacks fastest speed grade
- *Dedicated DSP48 Multiplier / Accumulator*
  - Up to 2000 DSP48 circuits support parallelism
  - Superset of the Virtex-5 DSP block
  - Pre-adder saves logic and power
    - improves performance
      especially for symmetrical FIR filters
  - ALU-like second stage reduces power



Virtex6

Select IO and Gigabit Transceivers

- *Select IO has higher performance*
  - LVDS @ 1.4Gbps, DDR3 @ 1066+ Mbps
  - Support for new memory types
    - DDR3-DIMM, RLDRAM-II, QDR-II+
- *GTX transceivers in every Virtex-6 device*
  - 150 Mbps to 6.5 Gbps, wide range @ low power
  - Generates less jitter, tolerates more jitter
    - Critical for CEI6, PCIe Gen 2, OC-48, OTU-1
  - Up to 72 Transceivers for highest bandwidth
  - Growing demand for popular standards above 3.75G
    - PCIe Gen2, SRIO2, CPRI/OBSAI 6G, CEI-6G, Interlaken, …
- GTH transceivers in the HXT family
  - highest speed: 11.2 Gbps,
  - Narrow-range LC-based VCO for lowest jitter

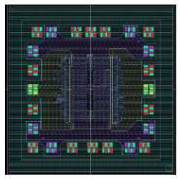
Virtex6

Dedicated Blocks for High-Bandwidth Standards

- *PCI-Express*
  - Now supports 5 Gbps Gen 2 (Spec 2.0): x1, x2, x4
    - Full Root Complex is supported with a soft IP wrapper
    - Allows simple FPGA to FPGA communication
  - Small wrapper for Endpoint implementation
    - Easier timing closure:
      <100 LUT for Virtex-6 FPGA vs. 3,000LUTs for Virtx-5 FPGA (x8)
- *EMAC*
  - *Ethernet at* 10/100/1000/2500 MHz
  - Stable standard; well understood use model
  - Very Similar to the Virtex-5 TEMAC block
    - Added 2.5G over-clocked mode (2500)
    - Demand for 2.5 G operation is growing
    - Interoperable with Broadcom ASSPs: 2.5 G switches

Virtex6

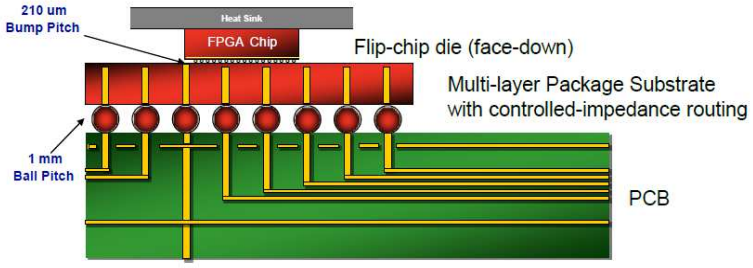
Attention to Signal Integrity Issues



- **Virtex-6 uses Flip-Chip technology**
- **I/Os spread over the chip,**
  - not limited to the periphery
  - No wire-bonded I/Os, less inductance
  - Up to 8000 micro-bumps attach to the package
- **Generous decoupling capacitors inside the package**
  - More effective, better quality, lower cost for the user
- **10-layer controlled-impedance package substrate**
  - 1-mm ball pitch to ease board layout
  - "Sparse Chevron" interspersed Vcc and GRD
  - Gigabit transceivers isolated on the left edge
  - Improved thermal performance,
  - metal top attached to the chip,
  - low thermal resistance to the board

Virtex6

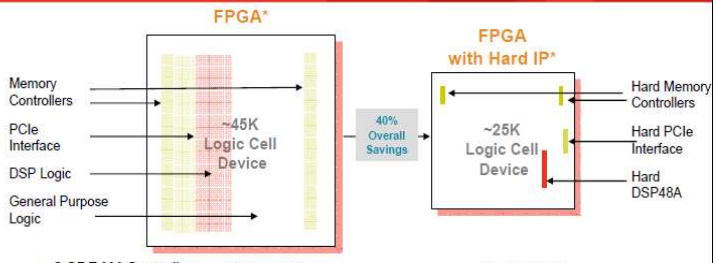
Virtex-6 Device Package Cross-Section



High-performance flip-chip technology Most designs are I/O-bound

Spartan6

Spartan-6 FPGA Big Cost Savings:
Hard Memory, DSP, PCIe Blocks



▪ 2 SDRAM Controllers	6K Logic Cells	Hard Block
▪ PCIe Interface	6K Logic Cells	Hard Block
▪ General Purpose Logic	22K Logic Cells	~24K Logic Cells**
▪ DSP (FFT, FIR, Symmetric TAP etc.)	11K Logic Cells	Hard Block
▪ Total	45K Logic Cells	24K Logic Cells

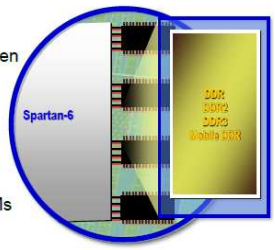
Hard IP Blocks Provide 80%+ Die Area Savings

High-End Features in Spartan-6 FPGAs

- **Spartan-6 uses a 45-nm process, optimized for low power**
  - Low-cost FPGAs usually sacrifice performance
  - But there are exceptions:
- **DDR3 Controller**
  - DDR3 is lowest cost external memory, but needs a demanding interface
  - DDR3 requires clock rate of >300 MHz (PLL on the memory device)
  - Spartan-6 devices incorporate 2 or 4 dedicated DDR3 controllers.
- **Multi-Gigabit Transceivers @ up to 3.125 Gbps**
  - For bit-serial connectivity between devices, boards and boxes
  - eliminates clock / data skew, reduces board area or cabling
  - differential signals, 4 wires total, support high-bandwidth traffic,

Integrated Memory Controller in Spartan-6 FPGAs

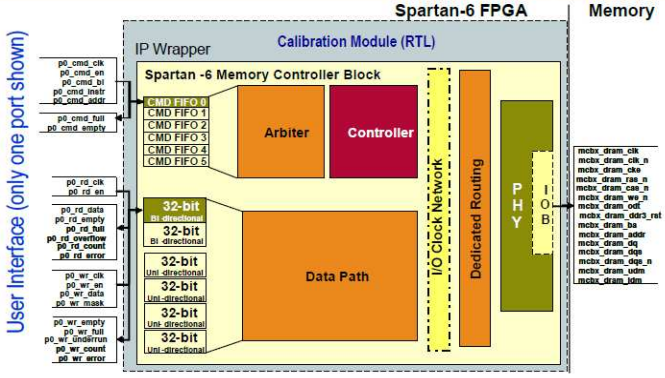
- **Provides interfaces from low cost FPGAs to industry's most popular DRAM memories**
  - DDR, DDR2, DDR3, mobile DDR
- **Up to 4 controllers in each Spartan-6 device**
  - Each of the these hard-coded controllers saves between 500 and 2000 LUTs versus soft solution
  - Very important for cost-sensitive designs
- **12.8 Gbps bandwidth per controller**
  - 16-bit wide, 400MHz / 800Mbps operation
  - Each controller interfaces to one DDR3 chip, no DIMMs
- **Fast and easy implementation**
  - Wizard guided design flow
  - Virtex-6 solution uses soft controller for flexibility



•**Low-cost FPGA meets low-cost, but fast memory**

Spartan6

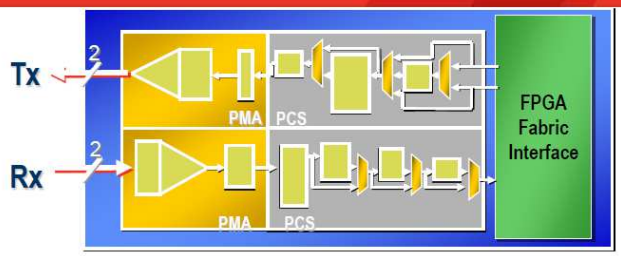
Memory Controller Block Diagram



- Simple user interface abstracts away complexity of memory transactions
- MIG / EDK wrapper delivers complete interface solution
  - Internal block assembly and signal connectivity is made transparent to the user

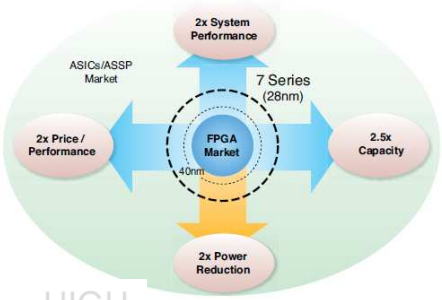
Spartan6

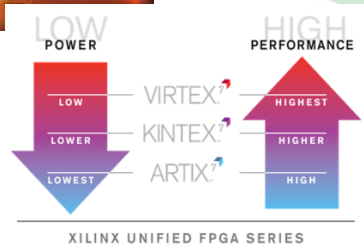
Multi-Gigabit Transceivers in Spartan-6 FPGAs



- Dedicated parallel-to-serial transmitter and serial-to-parallel receiver
  - Many programmable features, compatible with a wide range of standards
  - Unidirectional, differential bit-serial data I/O
  - Integrated PLL-based Clock and Data Recovery (CDR)
- Parallel interface to the FPGA internal fabric
  - 8 to 40 bit wide, to accommodate internal speed limits and optional fabric encoding
- Serial interface to the Printed Circuit Board (differential signaling)
  - Differential Current Mode Logic (CML)
  - Two traces for the transmitter, and two traces for the receiver, removes common-mode noise
  - Programmable signal swing and Tx & Rx equalization

7 Series





7 Series

ARTIX-7	KINTEX-7	VIRTEX-7
Lowest Power and Cost	Industry's Best Price / Performance "New Class of FPGA"	Industry's Highest System Performance and Capacity
Compared to Spartan-6 ▪ 2.4x larger ▪ 30% more performance ▪ 35% lower cost ▪ 50% less power ▪ 50% smaller footprint	**Compared to Virtex-6** ▪ Comparable performance ▪ 50% lower cost ▪ 50% less power **Compared to Spartan-6** ▪ 3.3x larger ▪ Over 2x performance with 4x transceiver speed ▪ Better Price / Performance	**Compared to Virtex-6** ▪ 2.5x larger (2M LCs) ▪ 50% lower power ▪ 2x line rate (28Gbps with 2.8Tbps serial bandwidth)

7 Series

7 Series
Breakthrough Power, Performance & Productivity

Maximum Capability	ARTIX-7 Lowest Power and Cost	KINTEX-7 Industry's Best Price/Performance	VIRTEX-7 Industry's Highest System Performance
Logic Cell Range	8K – 350K	70K – 480K	285K – 2,000K
Block RAM	18 Mb	34 Mb	85 Mb
DSP Slices	700	1,920	5,280
Peak DSP Perf.	375 GMACS	1,225 GMACs	3,368 GMACS
Transceivers	4	32	96
Transceiver Performance	6.6 Gbps	12.5 Gbps	13.1 Gbps 28 Gbps
Memory Performance	1,066 Mbps	2,133 Mbps	2,133 Mbps
I/O Pins	450	500	1,200
I/O Voltages	3.3V and below	3.3V and below 1.8V and below	3.3V and below 1.8V and below

7 Series

The Easy Way to Cost Savings

Xilinx EasyPath-6™ FPGAs offer a fast, simple and risk-free solution for cost reducing Virtex-6 FPGA designs. EasyPath-6 FPGAs deliver production volume devices in just six weeks with the lowest total product cost of any FPGA cost reduction solution. The cost savings are also available free of additional design constraints, re-engineering requirements, or re-layout of boards. EasyPath-6 FPGAs are architecturally equivalent to Virtex-6 FPGAs and match the FPGA datasheet specifications for functionality and timing. Unlike ASICs, the EasyPath-6 FPGA silicon requires no-requalification. Additionally, all Xilinx and third-party Intellectual Property (IP) for Virtex-6 FPGAs is supported by EasyPath-6 FPGAs without change or re-verification, and with no additional royalty, conversion or licensing fees.

COST REDUCTION OPTIONS

COST DRIVERS	EASYPATH-6 FPGA	STRUCTURED ASICS	STANDARD CELL ASICS
Time-to-Market	Fastest	Slow	Slowest
Design Effort/Cost	None	Medium	High
Re-Spin Risk	None	High	High
Qualification Costs	None	High	High
Opportunity Cost	None	High	Highest
NRE	Lowest	High	Highest

EasyPath FPGA

TIME-TO-MARKET COMPARISON

EasyPath FPGA 30..70 % cost FPGA