Dobre (☺?) praktyki inżynierskie – edytor schematów

Program wykładu

- Wprowadzenie
- Wybór/dobór elementów – kryteria
  - Dostawcy elementów na polskim rynku
- Schemat ideowy
  - Dobre praktyki przy pracy z edytorem schematów
  - Punkty kontrolne weryfikacji schematu (*check lists*)
  - Uczmy się na (cudzych..) błędach

Dobór elementów

Kryteria doboru elementów elektronicznych:

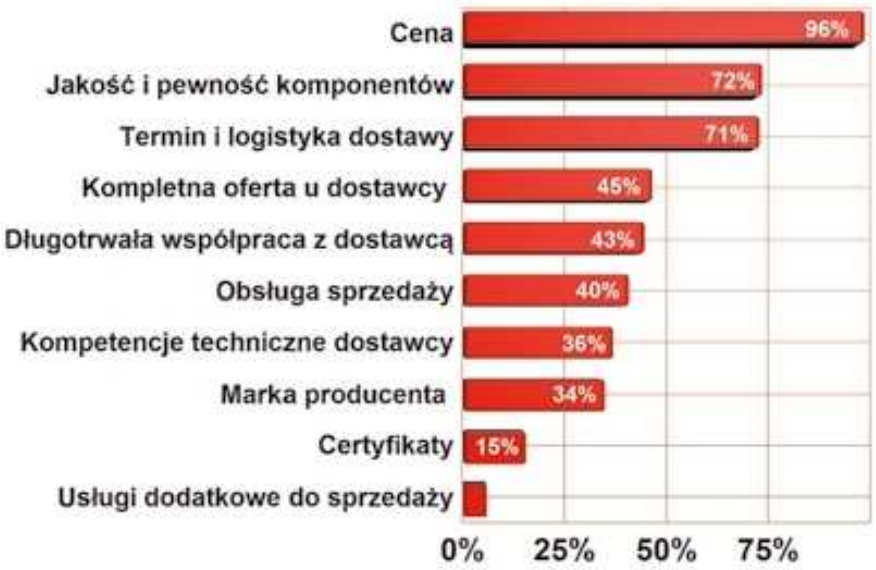
- ***funkcjonalność,***
- ***parametry (pracy, typ obudowy, wymogi środowiskowe),***
- ***dostępność (ew. zamienniki),***
- ***cena,***
- ***stabilność produkcji/ gwarancja dostaw,***
- ***historia stosowania,***
- ***wiarygodny dostawca.***

Dostawcy komponentów 2012 –ankieta

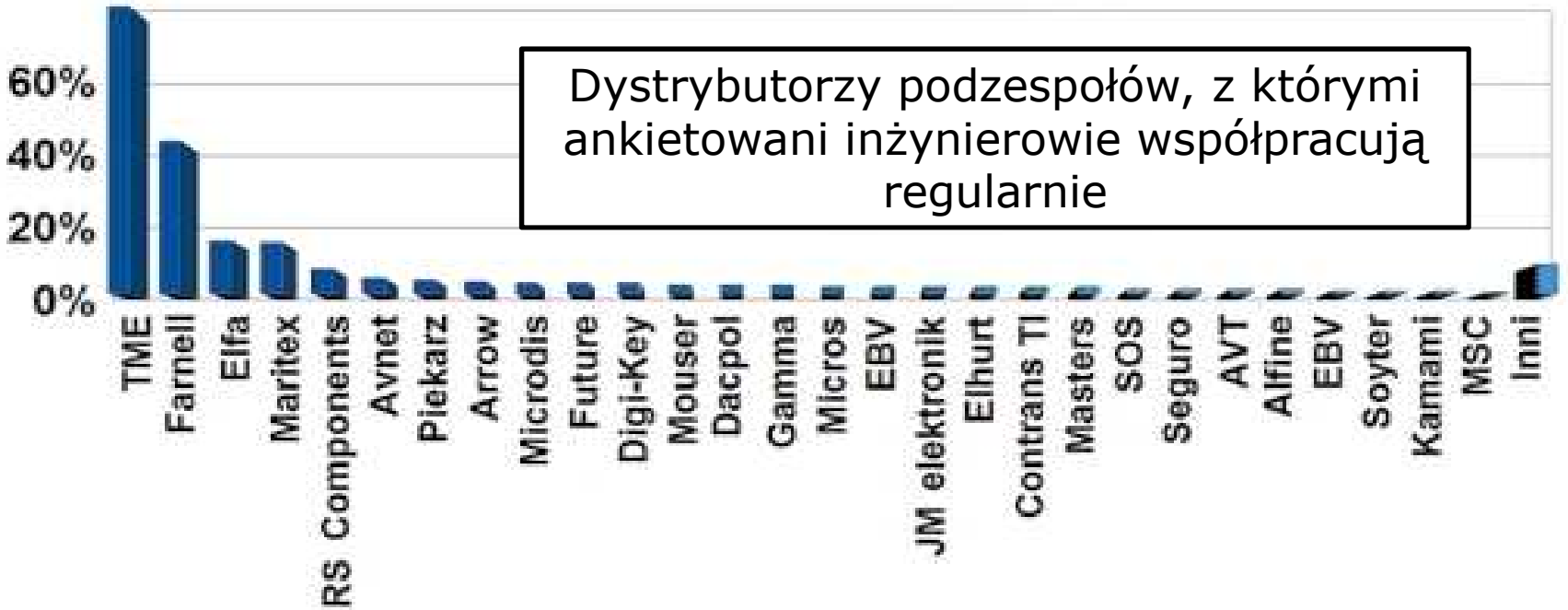
elektronikab2b.pl

Stanowisko pracy ankietowanych osób, których pytaliśmy o ich relacje z dystrybutorami

Co się liczy w ofertach handlowych najbardziej? Specjaliści odpowiadają zgodnie, że cena



Dostawcy komponentów 2012 –ankieta
elektronikab2b.pl



Dystrybutorzy podzespołów, z którymi ankietowani inżynierowie współpracują regularnie

http://elektronikab2b.pl/raporty/18327-podzespoly-elektroniczne-krajowy-rynek-dystrybucji

http://elektronikab2b.pl/prezentacja-artykul/27275-o-dwoch-takich-co-otworzyli-sklep-w-lodzi---a-teraz-sprzedaja-w-dzibuti#.VuFUrlvhDqk

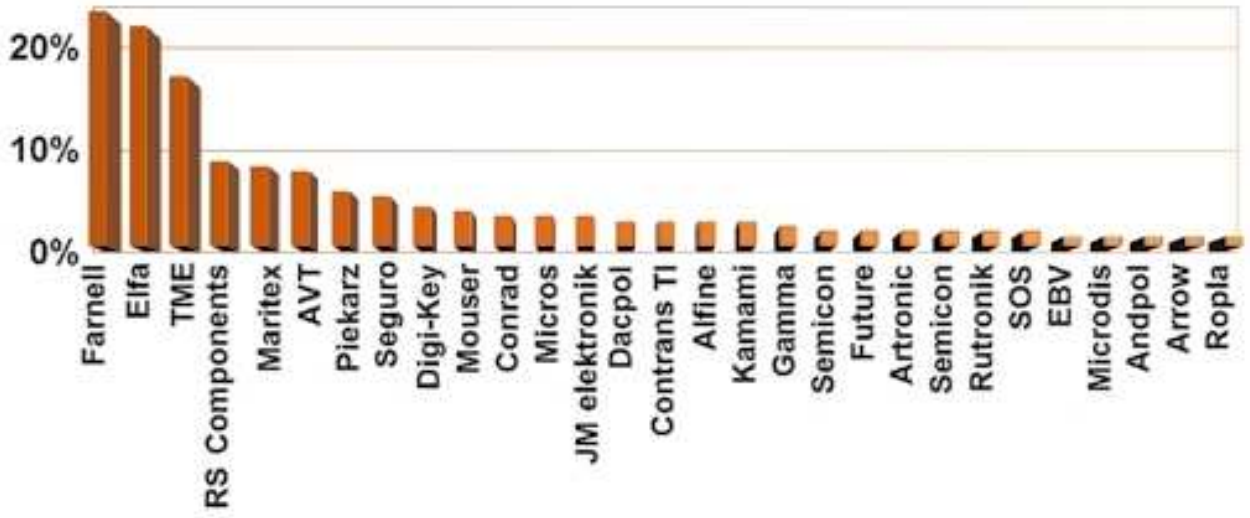
HISTORIA TME

Dostawcy komponentów 2012 –ankieta

elektronikab2b.pl

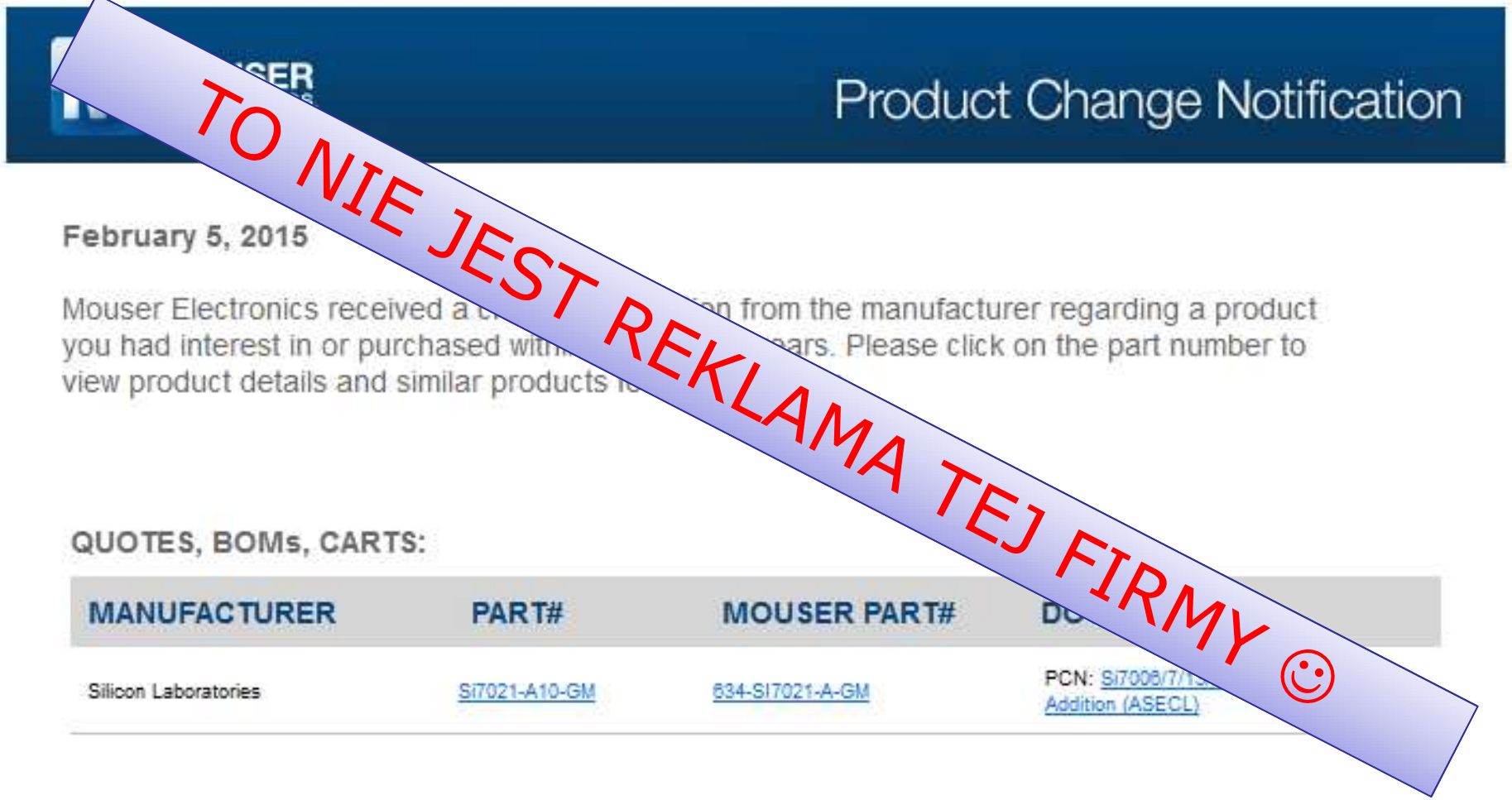
Jak często trafiasz na fałszywe komponenty - 39% pytanych zna ten problem z praktyki zawodowej

Dystrybutorzy podzespołów, u których zakupy są okazjonalne



JK1

Przyzwoici dostawy przysyłają dane PCN



Product Change Notification

February 5, 2015

Mouser Electronics received a [illegible] from the manufacturer regarding a product you had interest in or purchased with[illegible]ears. Please click on the part number to view product details and similar products [illegible]

QUOTES, BOMs, CARTS:

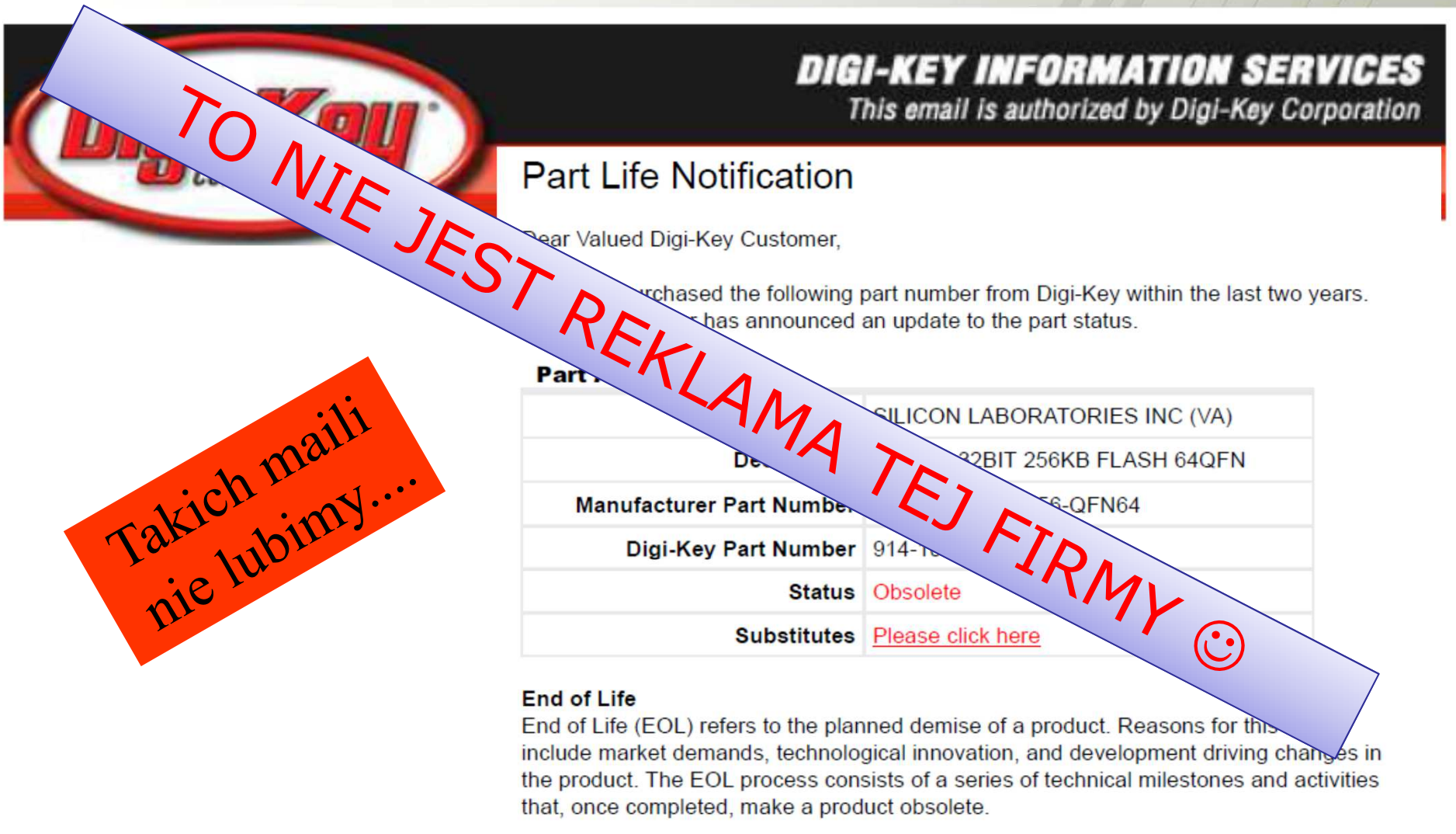
MANUFACTURER	PART#	MOUSER PART#	DC
Silicon Laboratories	SI7021-A10-GM	634-SI7021-A-GM	PCN: SI7006/7/13[illegible] Addition (ASECL)

TO NIE JEST REKLAMA TEJ FIRMY ☺

Slajd 7

JK1 Jerzy Kasperek; 2015-05-18

Przyzwoici dostawy przysyłają dane PCN



DIGI-KEY INFORMATION SERVICES
This email is authorized by Digi-Key Corporation

Part Life Notification

Dear Valued Digi-Key Customer,

...rchased the following part number from Digi-Key within the last two years. ...has announced an update to the part status.

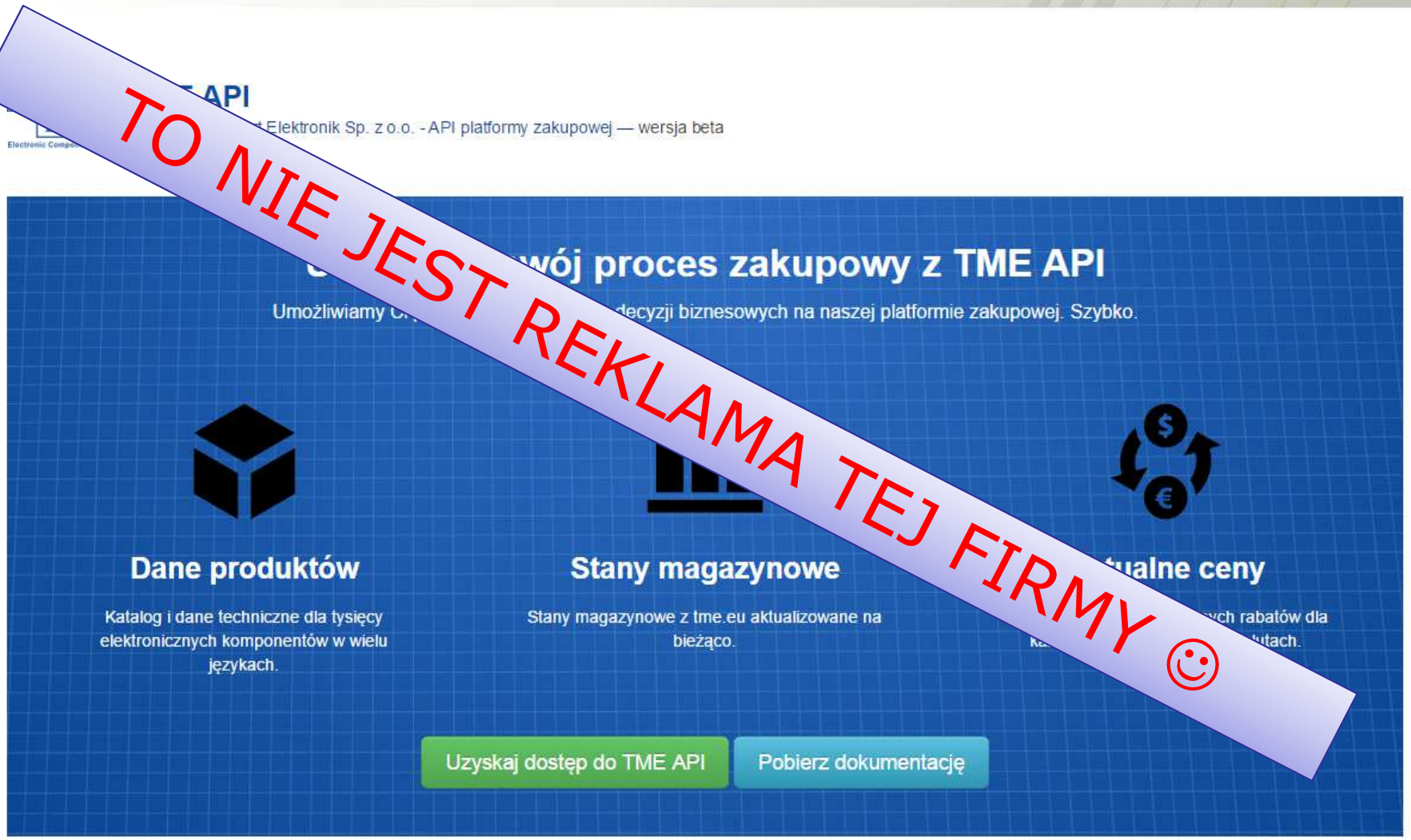
Part ...	
	SILICON LABORATORIES INC (VA)
De...	...32BIT 256KB FLASH 64QFN
Manufacturer Part Numbe...	...56-QFN64
Digi-Key Part Number	914-1...
Status	Obsolete
Substitutes	Please click here

End of Life
End of Life (EOL) refers to the planned demise of a product. Reasons for this include market demands, technological innovation, and development driving changes in the product. The EOL process consists of a series of technical milestones and activities that, once completed, make a product obsolete.

TO NIE JEST REKLAMA TEJ FIRMY ☺

Takich maili nie lubimy....

Przyzwoici dostawcy oferują API do swoich baz danych



TO NIE JEST REKLAMA TEJ FIRMY ☺

Dobre praktyki inżynierskie – schemat ideowy

http://electronics.stackexchange.com/questions/28251/rules-and-guidelines-for-drawing-good-schematics + komentarz JK

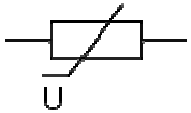
1. Use proper component designators

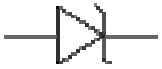
(czyli stosujemy normy ☺)

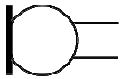
http://en.wikipedia.org/wiki/Reference_designator

IEEE 200-1975 - *IEEE Standard Reference Designations for Electrical and Electronics Parts and Equipments* (wycofany)

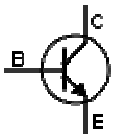
Obowiązuje ASME Y14.44-2008 (akceptowane przez IEEE)
+ IEEE-315-1975 *Graphic Symbols for Electrical and Electronics Diagrams (Including Reference Designation Letters)*

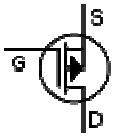


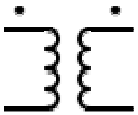




Jakie literki ?







Dobre praktyki inżynierskie – referencje

http://en.wikipedia.org/wiki/Reference_designator

Designator	
A	Separable assembly or sub-assembly (e.g. printed circuit assembly)
AT	Attenuator or isolator
BR	Bridge rectifier
BT	Battery
C	Capacitor
CN	Capacitor network
D	Diode (including LED, TVS, Thyristor, Zener)
DL	Delay line
DS	Display
F	Fuse
FB	Ferrite bead
FD	Fiducial
FL	Filter
G	Generator or oscillator
GN	General Network
H	Hardware, e.g., screws, nuts, washers
HY	Circulator or directional coupler
J	Jack (least-movable connector of a connector pair) | Jack connector
JP	Jumper (Link)
K	Relay or contactor
L	Inductor or coil or ferrite bead
LS	Loudspeaker or buzzer
M	Motor
MK	Microphone
MP	Mechanical part (including screws and fasteners)
P	Plug (most-movable connector of a connector pair) | Plug connector

Dobre praktyki inżynierskie – referencje

http://en.wikipedia.org/wiki/Reference_designator

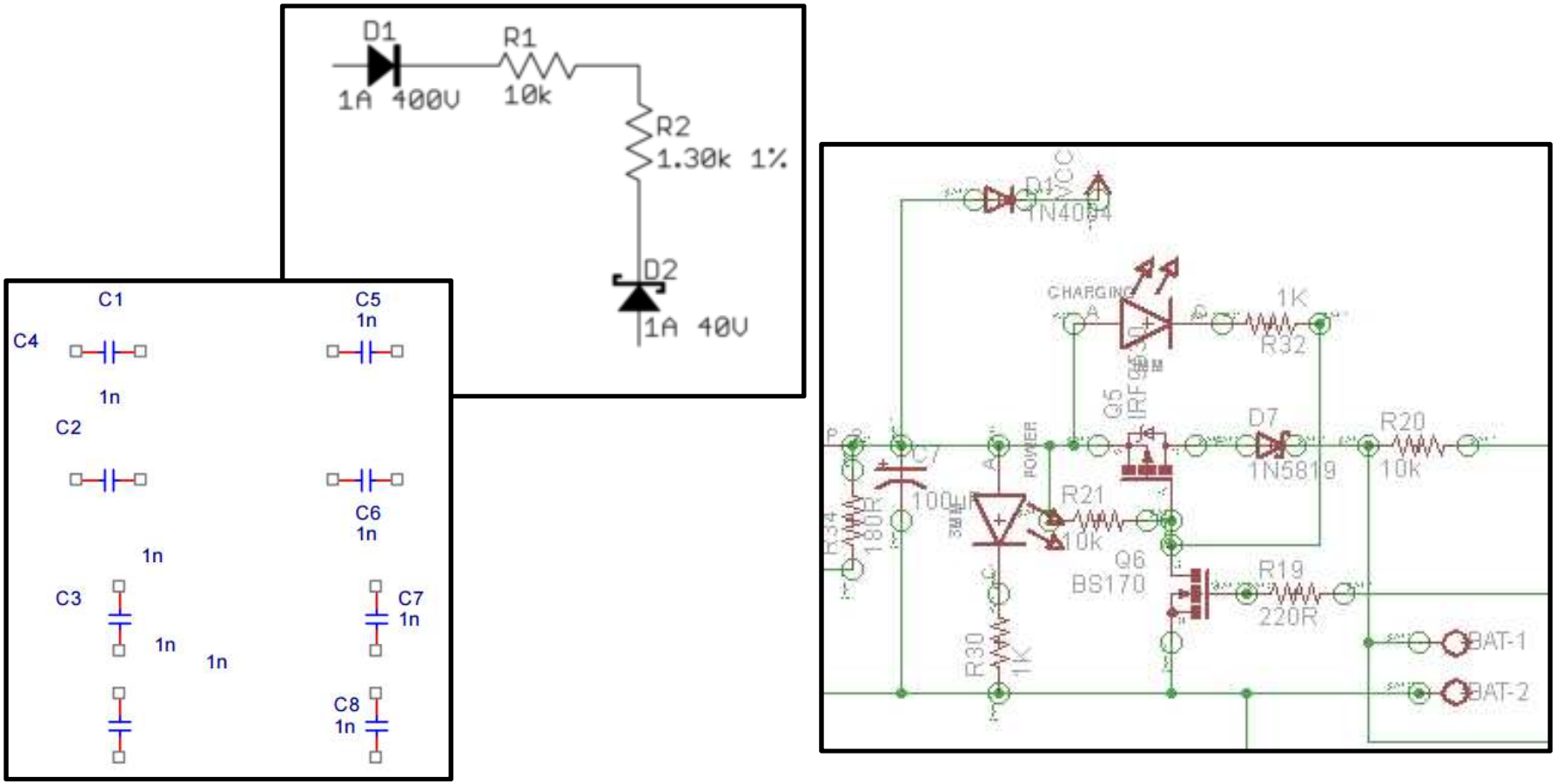
PS	Power supply
Q	Transistor (all types)
R	Resistor
RN	Resistor network
RT	Thermistor
RV	Varistor
S	Switch (all types, including push-buttons)
T	Transformer
TC	Thermocouple
TUN	Tuner
TP	Test point
U	Inseparable assembly (IC)
V	Vacuum tube
VR	Variable resistor (potentiometer or rheostat)

X	Socket connector for another item not P or J, paired with the letter symbol for that item XV for vacuum tube socket, XF for fuse holder, XA for printed circuit assembly connector, XU for integrated circuit XDS for light socket, etc.
Y	Crystal or oscillator
Z	Zener diode

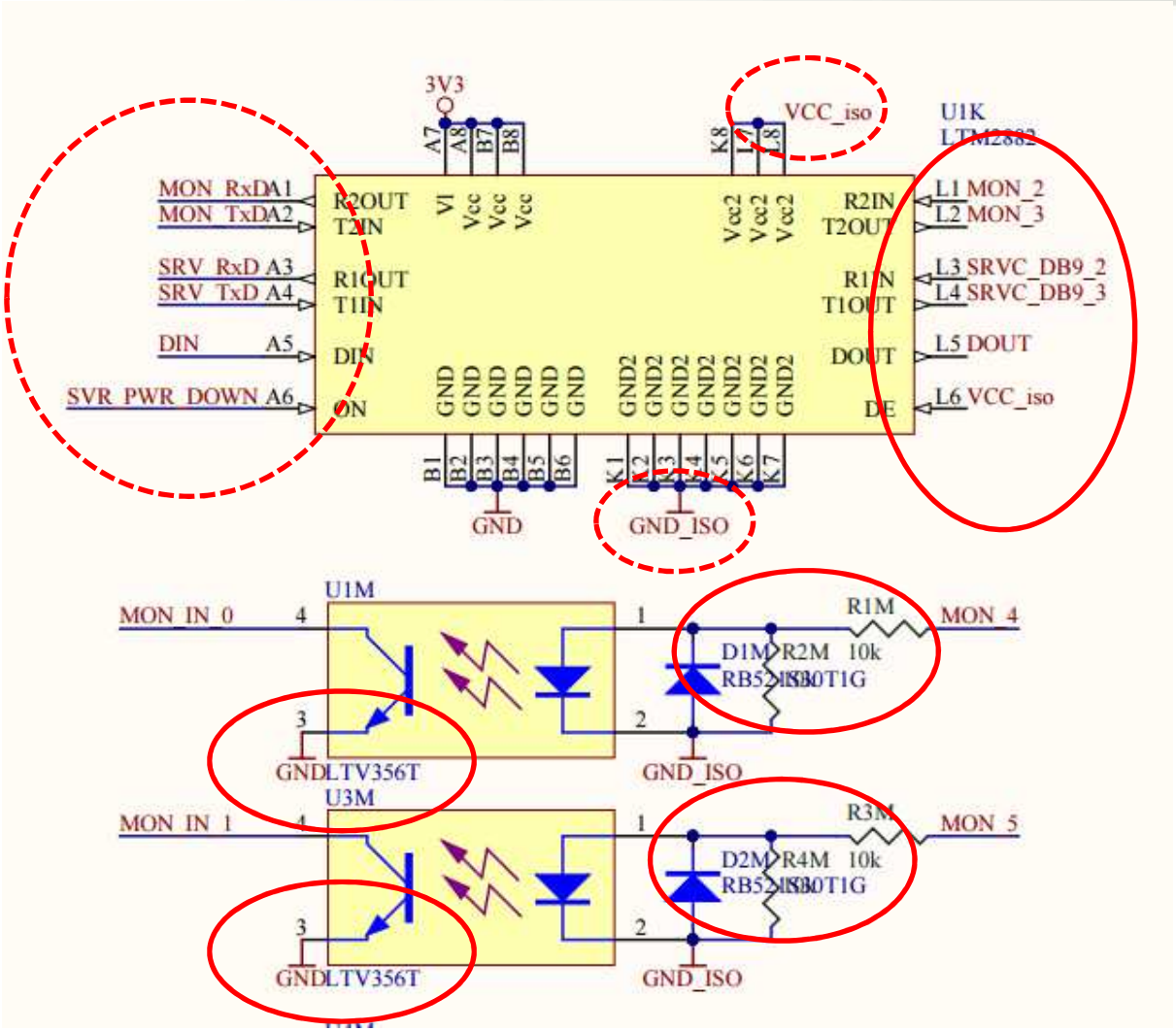
Dobre praktyki inżynierskie – schemat ideowy

http://electronics.stackexchange.com/questions/28251/rules-and-guidelines-for-drawing-good-schematics + komentarz JK

2. Clean up text placement



Dobre praktyki inżynierskie – schemat ideowy



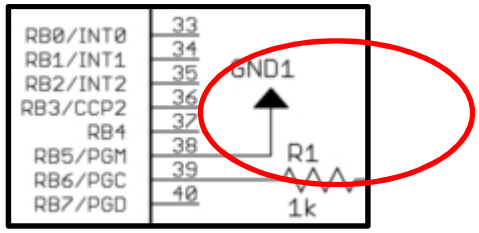
Wytęż wzrok ....

i znajdź odstępstwa od dobrych praktyk…

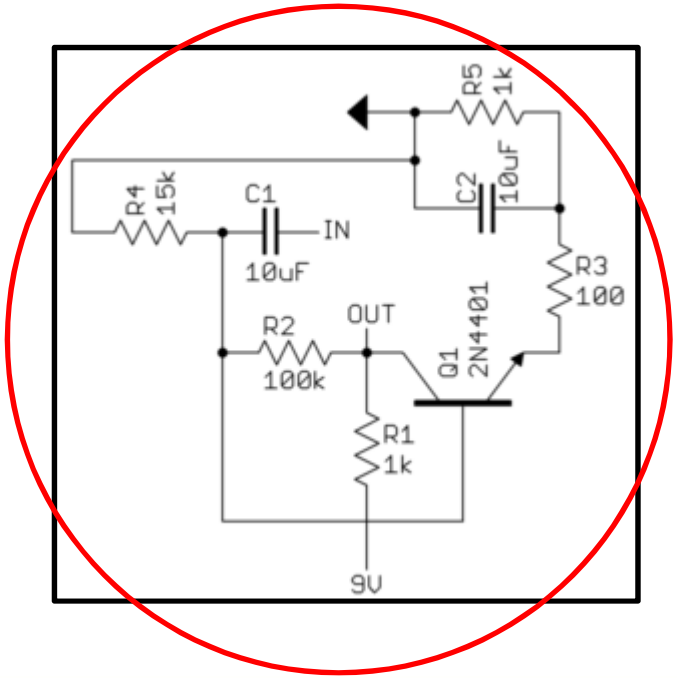
Dobre praktyki inżynierskie – schemat ideowy

http://electronics.stackexchange.com/questions/28251/rules-and-guidelines-for-drawing-good-schematics + komentarz JK

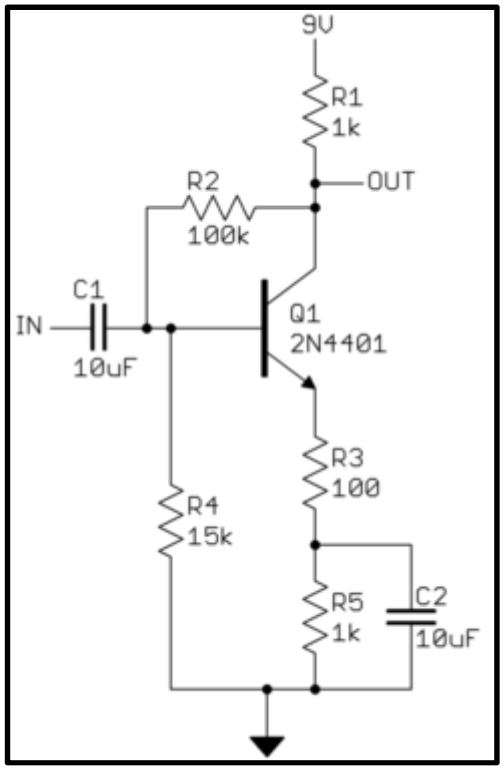
3. Basic layout and flowup



Zasilanie „w górę”
Masa „w dół”



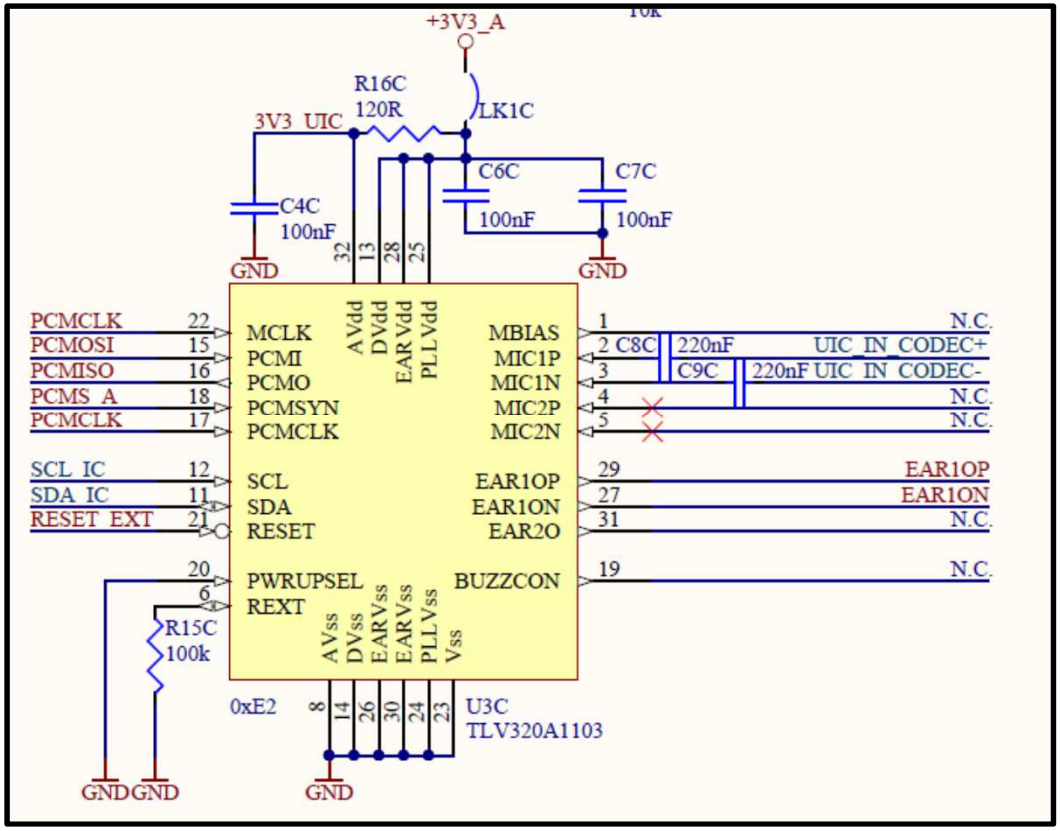
Układ lewo - prawo



Dobre praktyki inżynierskie – schemat ideowy

http://electronics.stackexchange.com/questions/28251/rules-and-guidelines-for-drawing-good-schematics + komentarz JK

4. Draw pins according to function

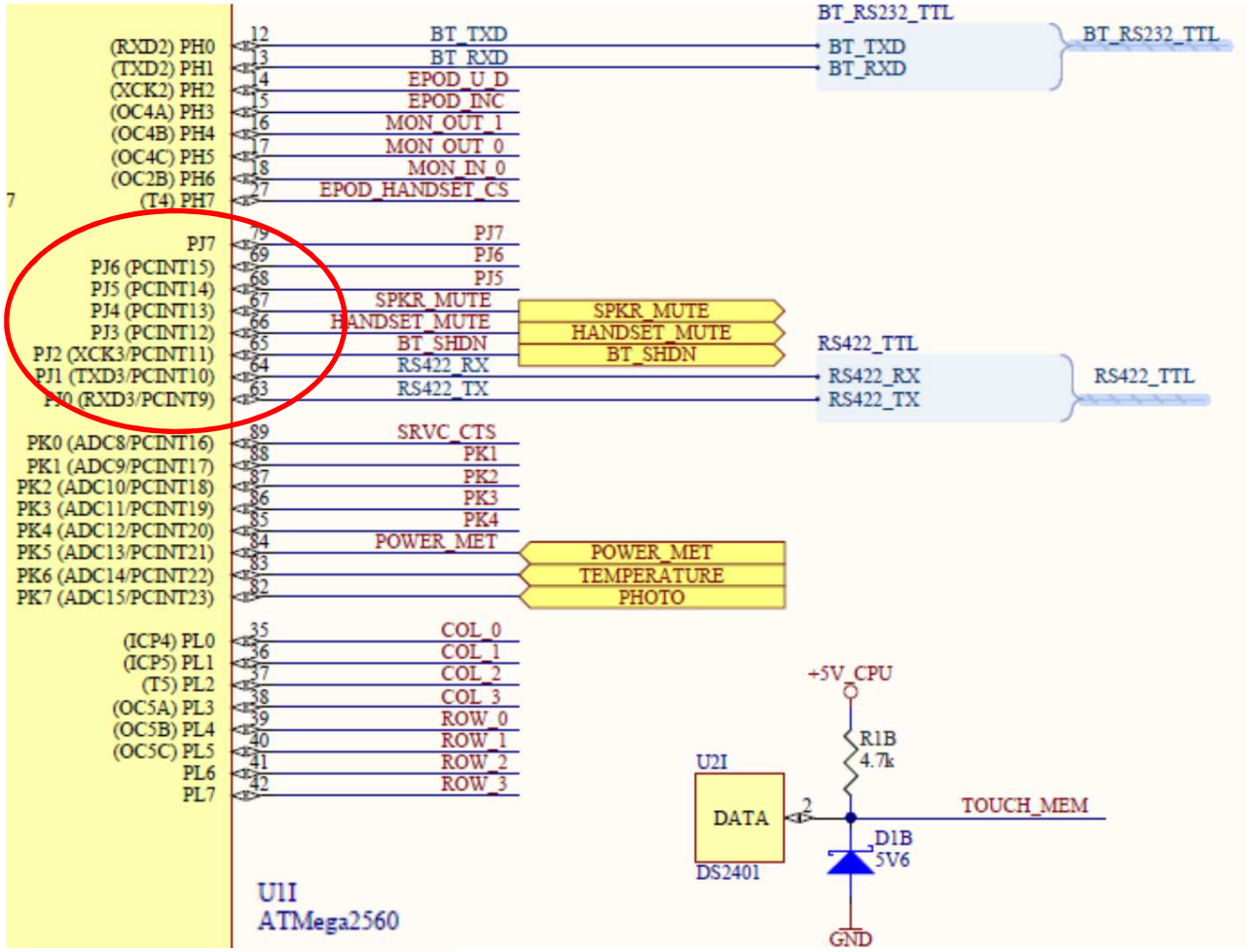


Niektórzy projektanci stosują porządek wyprowadzeń sygnałów zgodny z typem obudowy

–

motywując to łatwiejsze uruchamianiem PCB – ale to znacząco zaburza czytelność schematu

Dobre praktyki inżynierskie – schemat ideowy



Wytęż wzrok ....

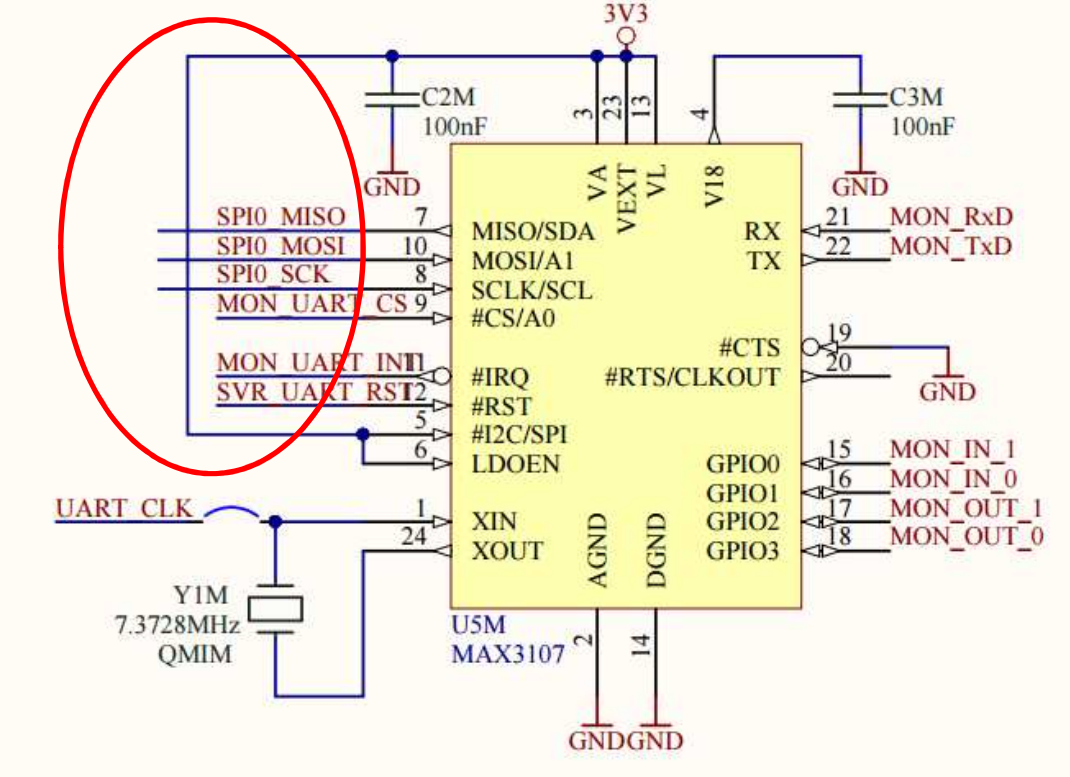
i znajdź odstępstwa od dobrych praktyk…

Porządek wyprowadzeń portu PJ inny niż pozostałych
- konsekwencja: zmarnowane 3h pracy programisty
☹

Dobre praktyki inżynierskie – schemat ideowy

http://electronics.stackexchange.com/questions/28251/rules-and-guidelines-for-drawing-good-schematics + komentarz JK

5. Direct connections, within reason



Używamy etykiet(y) ☺

Dobre praktyki inżynierskie – schemat ideowy

http://electronics.stackexchange.com/questions/28251/rules-and-guidelines-for-drawing-good-schematics + komentarz JK

6. Design for regular size paper

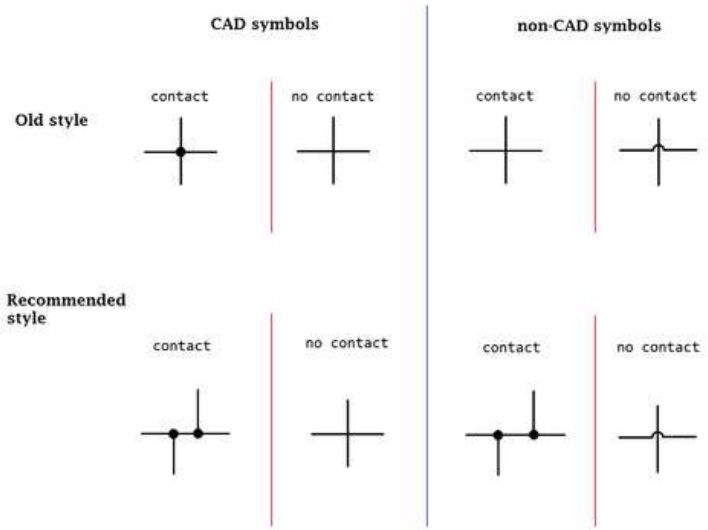
7. Labels key nets – 8.Keep names short

See this ANSI/IEEE standard for recommended pin name abbreviations.
http://www.altium.com/files/libraries/ls0001_pinabbreviation.pdf

9. Upper case symbol names

10.Show decoupling caps by the part

11.Dots connect, crosses don't



Altium

Pin Name Abbreviations

Summary

In certain instances, it may be desirable to abbreviate the pin names of schematic symbols. The following list contains commonly used abbreviations found in the Altium libraries.

Due to specific restraints and considerations, these mnemonics are not applied universally to every library component.

Library Standard
LS0001 (v1.2) March 19, 2004

Explanatory Notes

* Abbreviation from appendix A of ANSI/IEEE Std. 991 - 1986 (Current Nov 1996).

** Abbreviation conjoined as a prefix or postfix to an existing pin name.

Pin Abbreviations

Name	Abbrev. **	Name	Abbrev. **
Access	ACC	Antenna	ANT
Acknowledge *	ACK	Application	APPL
Acquistion	ACQ	Arbitration	ARB
Activate *	ACT	Asynchronous *	ASYNC
Activation	ACT	Asynchronous Preset-Enable	APE
Adder	ADD	Asynchronous/Synchronous	A/S
Address *	ADR A#	Audio	AUD
Address Latch Enable	ALE	Auto Reset	AR
Address Strobe	AS	Auto Zero	AZ
Adjust	ADJ	Auxiliary	AUX
Adjustment	ADJ		

Dobre praktyki inżynierskie – schemat ideowy

- Szablony firmowe
- Odpowiednie numery wersji / data z aktualnym numerem wersji arkusza (bloku funkcjonalnego) + numerem wersji PCB dla całego produktu (pole *Release*).

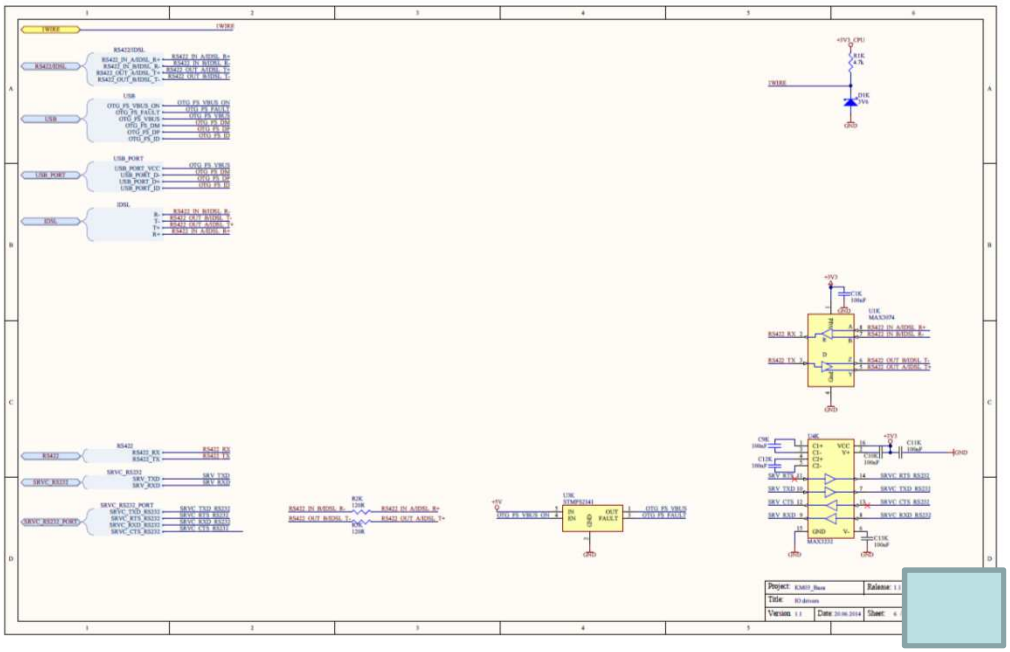
Title =title			=organization =address1 =address2 =address3 =address4
Size: A4	Number: =documentnumber	Revision: =revision	
Date: =CurrentDate	Time: =CurrentTime	Sheet =sheetnumber of =sheettotal	
File: =DocumentFullPathAndName			

Title Power			Altium Limited 3 Minna Close Belrose NSW Australia 2085
Size: A4	Number:	Revision:	
Date: 6/05/2009	Time: 10:18:35 AM	Sheet 5 of 5	
File: C:\Program Files\Altium Designer Winter 09\Examples\PCB training files\PCB training\Temperature Sensor\Power.SchDoc			

Bardzo częsty przypadek – nieczytelna domyślna tabelka np. z Altium ☺

Dobre praktyki inżynierskie – schemat ideowy

- Odpowiedni dobór rozmiaru do wielkości schematu.
- Centralne ułożenie elementów na schemacie.
- Etykiety / *harness* - wyrównane - w miarę możliwości taka sama szerokość *harness* - zwłaszcza jeżeli występują obok siebie
- Bloki funkcjonalne (*sheet*) wyrównane i w odpowiednich wymiarze.

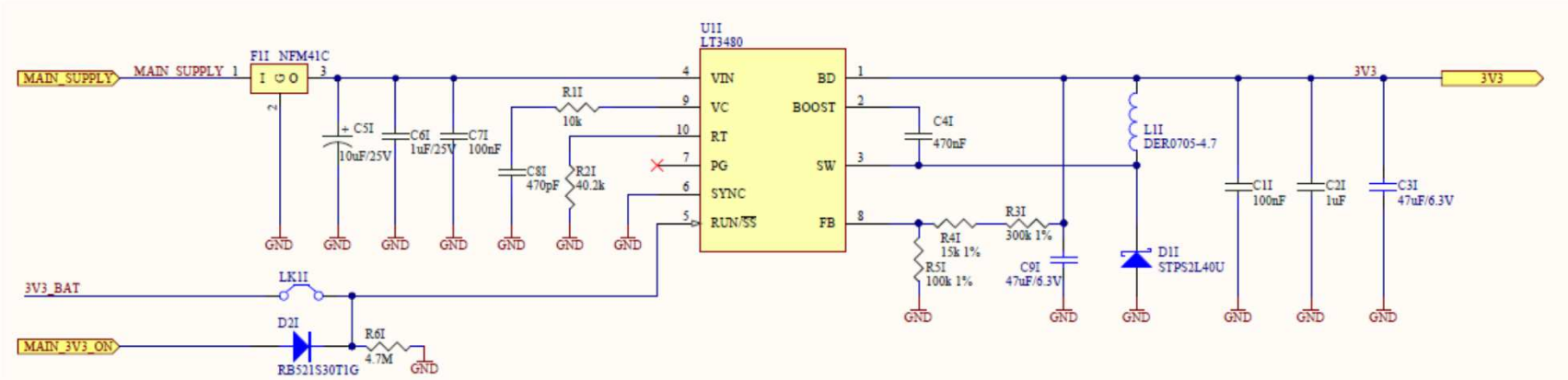


Dobre praktyki inżynierskie – schemat ideowy

- Wszystkie niewykorzystane wyprowadzenia z układów scalonych złącz itp. itd. etykieta N.C. (NO ERC)
- W miarę możliwości - zachować regułę przepływu sygnałów z lewej strony na prawą.
- W schematach hierarchicznych, o ile to możliwe zachować położenie portów wejściowych po lewej a wyjściowych po prawej stronie schematu.
- W schematach hierarchicznych unikać rysowania portów bezpośrednio przy układach scalonych - stosować technikę port + etykieta z boku schematu i etykieta + przewód przy układzie scalonym.
- Czytelność - każdy napis nie może być przekreślony np. przewodem – wskazane jest aby napis był odsunięty od pozostałych symboli na schemacie.
- Unikamy zagęszczeń elementów/symboli.

Dobre praktyki inżynierskie – schemat ideowy

- Wyrównanie elementów np. połączeń do masy, symetryczne położenia elementów.
- Każda etykieta połączona z przewodem - unikać sytuacji łączenia etykiety np. z wyprowadzeniem z układu scalonego bez przewodu.
- Takie same elementy (np. etykiety / przewody) w tym samym kolorze.
- Położenie etykiet - poza obrysem elementu taka sama etykieta nie powinna „wisieć” w powietrzu czyli wychodzić poza przewód.
- Oznaczenie max napięcia pracy dla zastosowanych kondensatorów np. 100nF/50V.
- W SVN danego projektu tylko pliki źródłowe aktualne w danej wersji.



Dobre praktyki inżynierskie – schemat ideowy
- check lists http://www.aqdi.com/check.htm
(C) 2003 Hank Wallace

This is a checklist for electronics designers. The idea is for engineers and technicians to share experiences and create a detailed checklist which the individual designer can pare down to meet his or her specific needs. There are many details that go into the making of a first-run design success, and this checklist helps prevent Murphy's gremlins from marring an otherwise healthy design.

How do you use this checklist?

Make a copy of the list on your computer. Edit the rules to conform to your company's practices and delete the rules that do not apply to your work.

Discuss the checklist with others you work with, adding items from their experience. For maximum benefit, get their commitment to use it, too.

Make the checklist part of your design review and design release procedures. Do not release a product for prototyping or manufacturing until each checklist item has been verified.

Keep the original checklist for each release or revision so you can close the loop on the process, adding some items later if needed. For each design error that occurs, add an item to the list.

Contribute your suggestions for additions or changes so others can benefit from your experience. Suggestions? Go to www.aqdi.com and send feedback.

***THANKS** to all the readers who have contributed to this checklist over the years. You have helped reduce the incidence of **gastrointestinal distress** among engineers worldwide.*

Dobre praktyki inżynierskie – schemat ideowy
- check lists http://www.aqdi.com/check.htm
(C) 2003 Hank Wallace

- *all unused inputs terminated*
- *race conditions checked*
- *Darlington outputs (1.2v low) driving logic inputs*
- ***mating connectors on different assemblies checked for same pinout***
- ***all outside world I/O lines filtered for RFI***
- ***all outside world I/O lines protected against static discharge***
- *bypass cap for each IC*
- *voltage ratings of components checked -- as was not done in the on-board computer in my 1990 Geo Tracker, apparently manufactured by Mitsubishi, where capacitor C4 was rated at 47uf/50V across an automotive rail which can easily see larger spikes. Other owners reported such problems in vehicles from 1990 to 1995, with the capacitor spewing electrolyte onto the conformally coated PCB, corroding conductors in the vicinity. Hats off to Mitsubishi for ignoring a simple checklist item for five years and who knows how many hundred thousand vehicle shipments, and who knows how many in-service failures.*
- *each IC has predictable or controlled power-up state*
- *file name on each sheet*
- *dot on each connection*
- *minimum number of characters in values (100n/?/100nF 100/?/100R)*
- *consistent character size for readability*
- *schematics printed at a readable scale*
- *all components have reference designators and values*
- *special PCB or parts list information entered for each component, if required*

Dobre praktyki inżynierskie – schemat ideowy
- check lists http://www.aqdi.com/check.htm
(C) 2003 Hank Wallace

- *electrolytic and tantalum capacitors checked for no reverse voltage*
- *power and ground pins listed for each component with hidden power pins*
- ***check hidden power and ground connections***
- *title block completed for each sheet*
- *ground made first and breaks last for hot pluggability*
- *pullups on all open collector outputs*
- *sufficient power rails for analog circuits*
- *LM324 and LM358 outputs loaded to prevent crossover distortion*
- ***amplifiers checked for stability***
- *oscillators checked for reliable startup*
- *consider signal rate-of-rise and fall for noise radiation*
- *check for input voltages applied with power off and CMOS latchup possibilities*
- *reset circuit design reliable, both glitch-free and consistent; tested with slow power supply fall time*
- *separate analog signals from noisy or digital signals*
- *ability to disable watchdog timer for testing and diagnostics and emulation*
- *sufficient capacitance on low dropout voltage regulators*
- *setup, hold, access times for data and address busses*
- ***check the data sheet fine print and apnotes for weird IC behaviors***
- *determine effect of losing each of multiple grounds on a connector*
- *automotive powered devices must withstand 60 to 100 volt surges*
- *check maximum power dissipation at worst-case operating temperatures*
- *check time delays and slew rates of opamps used as comparators*

Dobre praktyki inżynierskie – schemat ideowy
- check lists http://www.aqdi.com/check.htm
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- *check opamp input over-drive response for unintended output inversion*
- *check common mode input voltages on opamps*
- *check for voltage transients and high voltages on FET gates*
- ***check failure modes and effects of failed power semiconductors***
- *estimate total worst case power supply current*
- ***check pin numbers of all custom-generated parts***
- *for buses, ensure bus order matches device order*
- *ensure resistors are operating within their specified power range plus safety factor*
- *resistor power ratings derated for elevated ambient temperatures*
- ***electrolytic/tantalum capacitor temperature/voltage derating sufficient for MTBF***
- *check for low impedance sources driving tantalum caps which can cause premature failure*
- *avoid reverse base-emitter current/voltage on bipolar transistors*
- *use of baud rate friendly clock source for devices that have serial ports*
- *~IOR and ~IOW strobes on UARTs are typically incompatible with timings of signals readily available on many processors*
- *ROHS compliance requirement review*
- *part obsolescence review*
- *replacement part compatibility with software requirements: "top-boot vs. bottom boot FLASH", UART compatibility, SPI memory timing and addressing for different sized parts*
- ***all PCB signal changes noted to the software developers (JK:jeden soft dla kolejnych wersji)***
- *all no-connect pins on IC's should be labelled NC*

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- ***text should not overlap wire or symbol graphics on schematics***
- *busses with off-page destinations present with title at page margin*
- *card edge connectors identify mating part*
- *page title present and consistent on all pages if not in title block*
- *under-utilization of gates on multi-gate parts checked*
- *off board connectors identify all signals even if not used on this design*
- *unpopulated parts annotated and enclosed by dashed-line box on schematics*
- *wires exist between all connected pins/ports (no direct pin/pin connections) if capture package does not like such connections*
- *symbols identify open collector/drain pins and internal pulled up/down pins*
- *clock lines with series termination and parallel termination component locations present even if not populated; zero ohm resistor for series, unpopulated parts for parallel termination*
- *avoid direct connect of mode pins or no-connect bus lines to GND or VCC so PCB rework options are maximal*
- *diagnostic resources by design (leds, serial ports, etc.) even if unpopulated by default*
- *pin names and attributes on symbols with multi-function pins should match actual design usage (I/O/Bi, Name)*
- *connect DIP switches and other grouped I/O to ports in a logical way, LS bit to LS bit, MS bit to MS bit*
- *piezo elements generate voltages (when shocked) that can destroy their drivers -- check for susceptibility*
- *preferred component reference designators*

Dobre praktyki inżynierskie – schemat ideowy

http://electronics.stackexchange.com/questions/6644/good-schematic-checklist

- *Do all tantalum caps on rails have at least ~20% overhead? No 25V caps on 24V lines?*
- *Are there bypass caps on the power rails of every chip? Even the ones that don't look like chips, like regulators?*
- *Are there filters on every transistor gate/base? Even the ones in processors?*
- *Are there filters on A/D converter pins?*
- *Are there pullups or pulldowns on every pin where it could matter? Look especially for diodes driving processor inputs or transistor gates, or hanging off an input to the board. Also, outputs of comparators.*
- *Is there impedance on every pin feeding directly into a processor from off-board? A transistor?Something to eat noise and keep it from frying your chip?*
- ***Do you have test points on all rails and signals of interest? Including at least one debug pin off any processor?***
- ***Is there an LED to indicate power to the board? A second LED, processor controlled, for blink codes?***
- *Is there too much cap on any power rail? Switching regulators have a limit on how much cap they can pull up.*

STEPHEN COLLINGS
I spec and design power stages, PCBs, and embedded microprocessor controls for 5kW-1000kW power converters.
@swcollings

Dobre praktyki inżynierskie – schemat ideowy

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- *Are all op-amps negative feedback, and all comparators positive feedback? (Obviously there are exceptions to this, I just find it a useful basic rule to check in my applications.)*
- *Are all op-amp and comparator power rails connected in the correct polarity?*
- *Are there any capacitors or zeners directly on the output of an op amp? Should be impedance between.*
- *Are all unused op-amps and comparators tied down properly? Tie op-amp outputs to the negative input, and tie the positive input to common. Tie to common all pins on an unused comparator.*
- *Do all optocouplers have resistors and caps in parallel with their diodes, for noise immunity?*
- *Make sure all user accessible power rails are short-circuit protected.*

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Functionality:

- *Check symbol pinouts, especially for new symbols and parts with multiple packages.*
- *Review vendors' latest data sheets and errata to see if anything has changed since you downloaded it.*
- *Have the vendor's FAE review the part of the schematic that uses their part(s)*
- *Label all power nets consistently. Makes it easier to find them during the PCB design.*
- *Check for on- and off-page connections, using the tool's DRC.*
- *Check for same net on different pages without on/off page, using DRC.*
- *Avoid strange symbols (e.g. #) that other tools may not handle well.*
- *All upper case.*
- *Show revisions. Show when drawn, whom by.*
- *Think about EMI/EMC/FCC/UL/CE, etc.*

BRIAN CARLTON
MANAGER, HARDWARE DEVELOMENT. ALSO PROJECT MANAGEMENT, LEAD, AND FPGA WORK. PROGRAMMING IN VHDL AND VERILOG (FOR FPGAS) AND PERL (FOR TOOLS).

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Ease of use:

- *No 4-way ties.*
- *Label all important nets, e.g. clocks, power even if only going between 2 chips. Makes checking if the clock's serial termination resistor is near the clock driver. Also good for high-current signals that aren't the main power rails, e.g. around the FET or inductor in a DC/DC switcher.*
- *Table of contents on an early page; block diagram on an early page.*
- *Show power and ground on schematic symbols.*
- *Show unused gates/resistors from multi-gate/resistor packages.*
- *Show active low pins on symbol; show active low nets consistently.*
- *No extra connection dots where there isn't a connection.*
- *Not larger than B-sized (11x17) or metric equivalent.*
- *Bus common signals.*
- *Connect by name on-page if it makes it more readable. Similarly don't wire power/ground all over the page, use multiple power/ground symbols.*
- *Inputs on the left, outputs on the right.*
- *Everything on a grid.*

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Uczmy się na błędach (najlepiej cudzych ☺)

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Kilka lat utrzymania produktu….

Typowe komunikaty o poprawkach:

- Wartości elementów - parametry środowiskowe + temat unifikacji
- Inna funkcjonalność – zmiany w schemacie ideowym
- EMC – duuuży temat ☺
- Analiza FMEDA – duuuży temat ☺
- Zamienione sygnały magistrali szeregowych (TxD RxD, I2S, SPI)
- Czytelność schematu ideowego
- Różne błędy PCB (temat na osobny wykład…)
  - poprawki *layout*-ów elementów – sprawdzenie każdego nowego elementu bibliotecznego
  - błędy w dokumentacji montażowej elementów PCB (np. odwrócone LEDy, niejasna polaryzacja kondensatorów tantalowych)
  - mechanika – montaż, dostęp serwisowy itp. (+ciekawostki: np.: zatrzaski gniazda ETH szorują po PCB)

Koniec ....