



Platforma sprzętowa

- **Architektura układów FPGA**

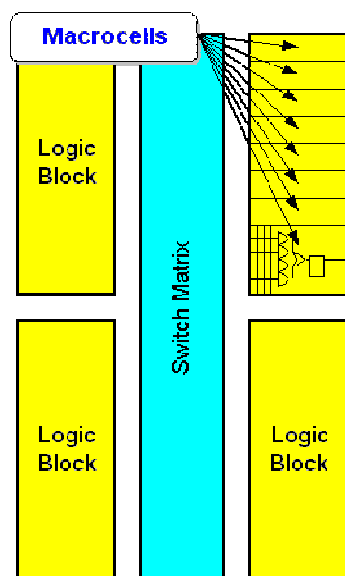
- **Rodzina Xilinx Artix-7**



- **Platforma Digilent Nexys4**



Architektura układów FPGA CPLD kontra FPGA



typu PAL
więcej logiki kombinacyjnej

mała / średnia
wielokrotna struktura 22V10

do ~300 MHz
przewidywalne opóźnienia

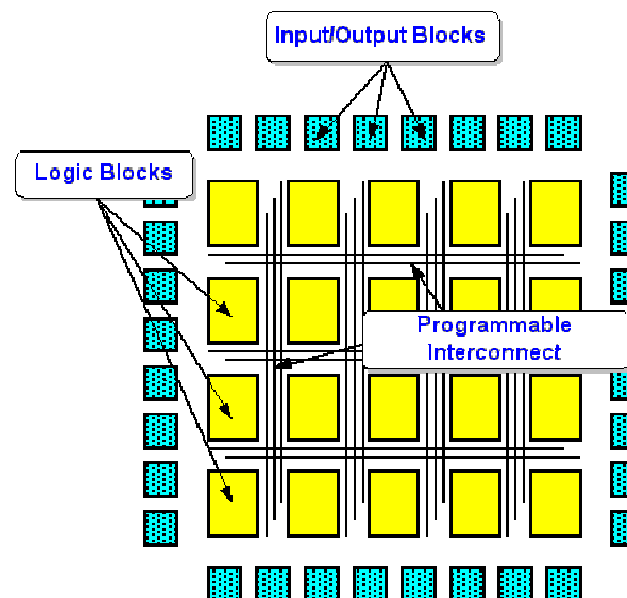
macierz łączeniowa

ARCHITEKTURA

GĘSTOŚĆ

SZYBKOŚĆ

POŁĄCZENIA

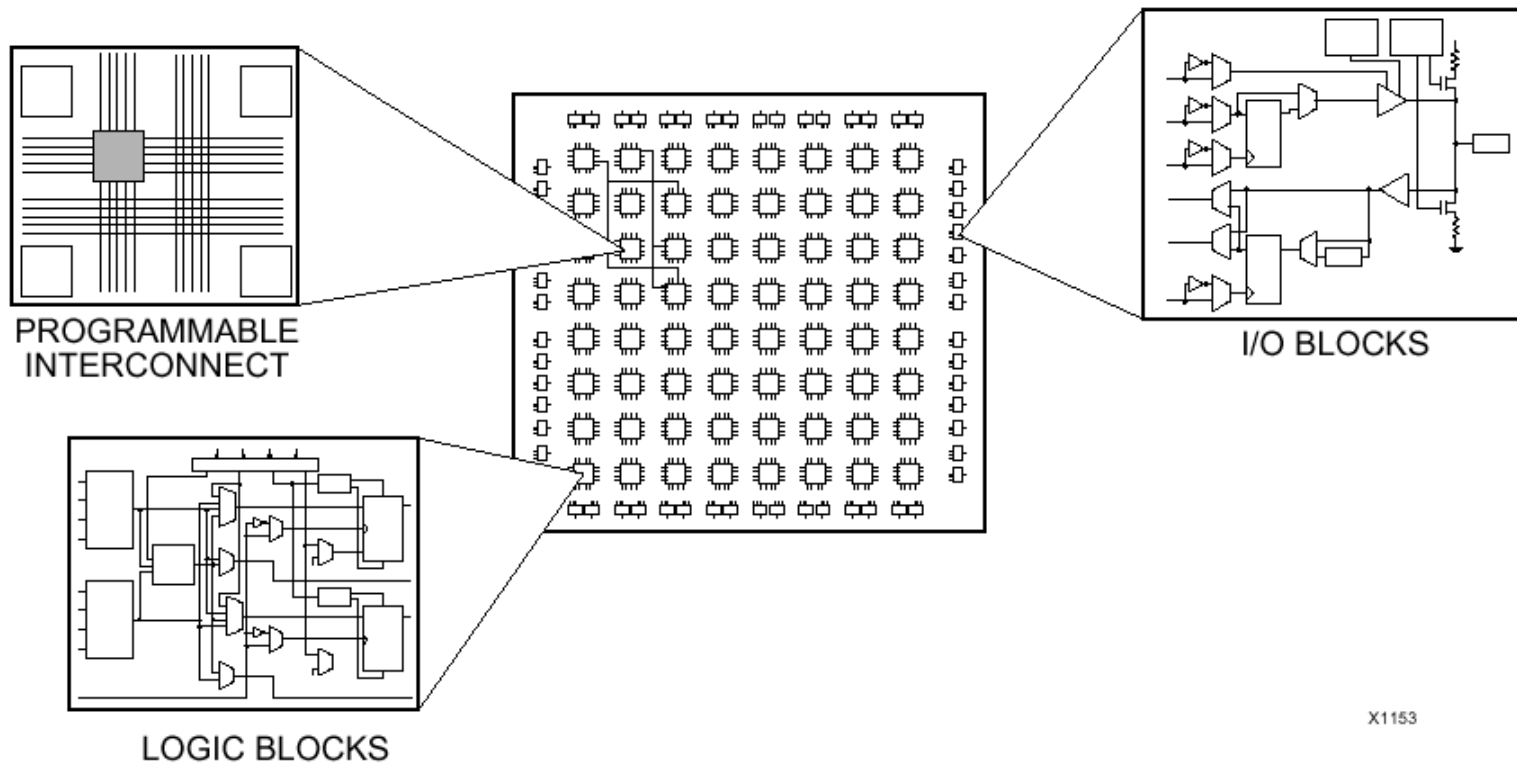


typu Gate Array
więcej przerzutników

średnia / duża / bardzo duża
do 10 milionów bramek

do ~1000 MHz
opóźnienia zależne

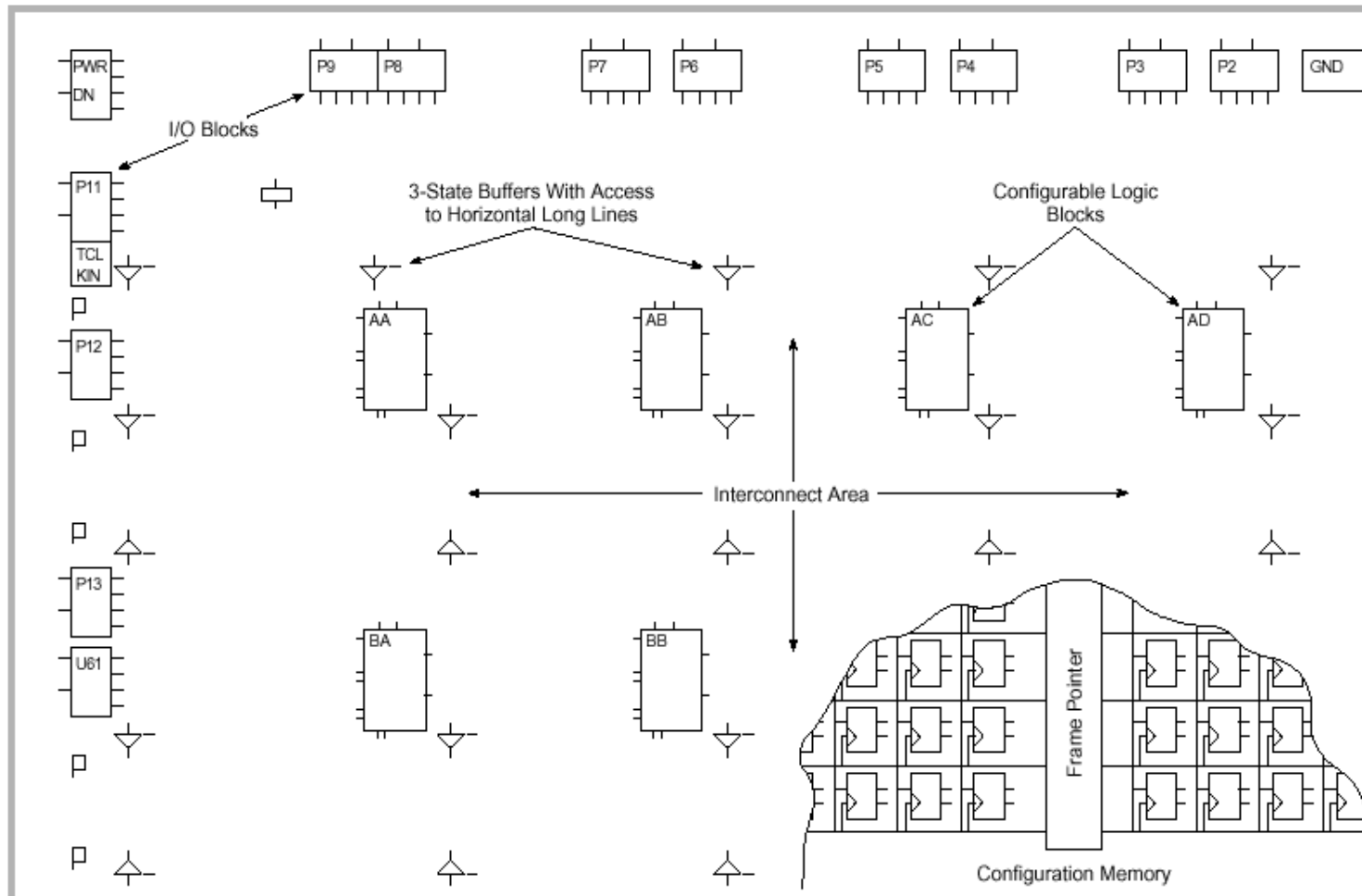
połączenia odcinkami



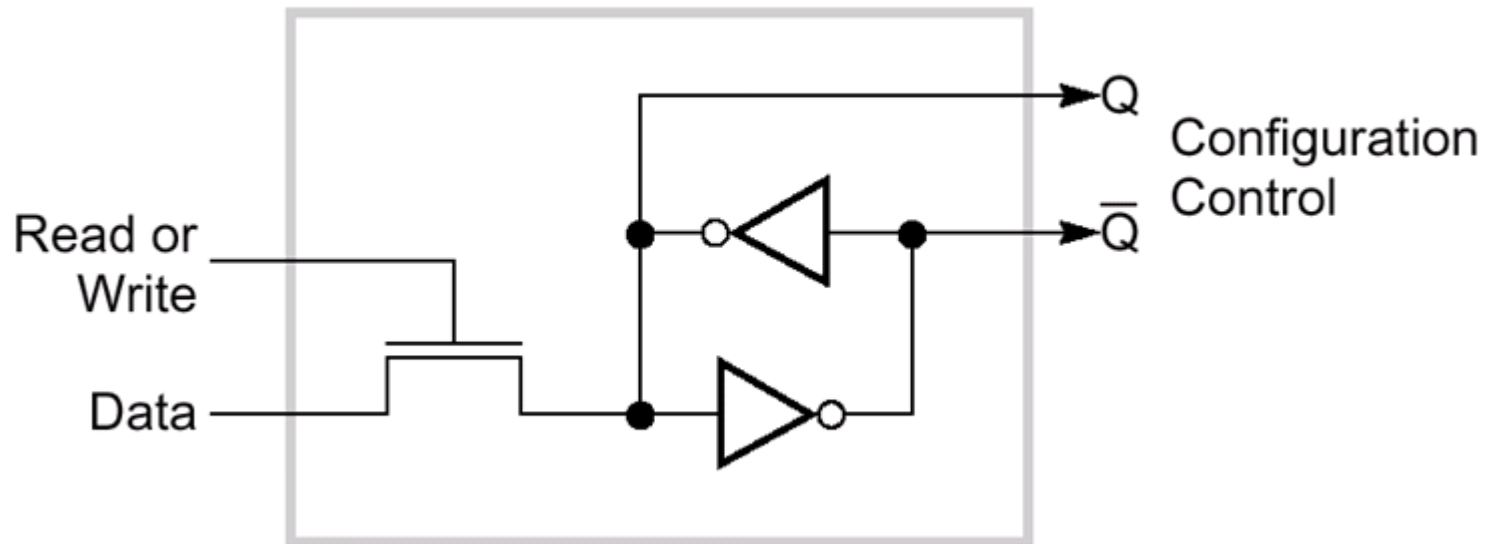
- **Bloki we/wy** (*Input Output Block*)
- **Bloki logiki** (*Configurable Logic Block* i inne specjalizowane)
- **Zasoby połączeniowe** (*Logic Interconnect*)

Architektura układów FPGA

Zasoby użytkowe a pamięć konfiguracji

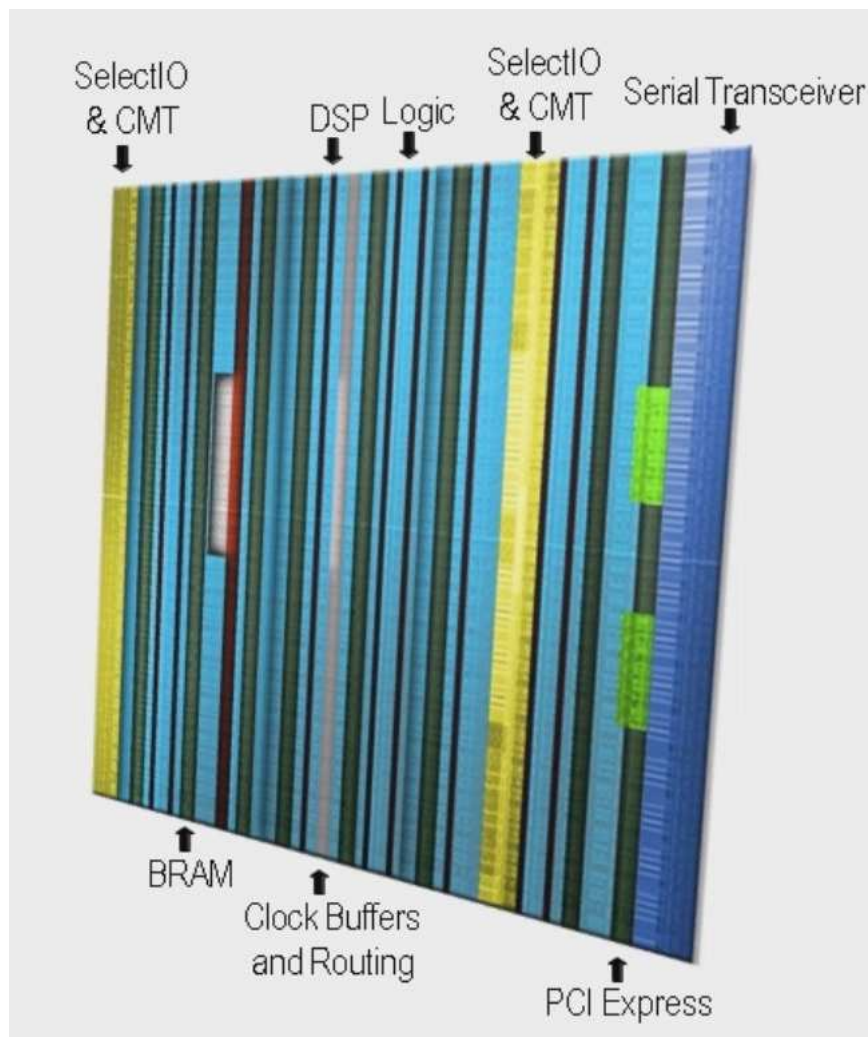


X3241



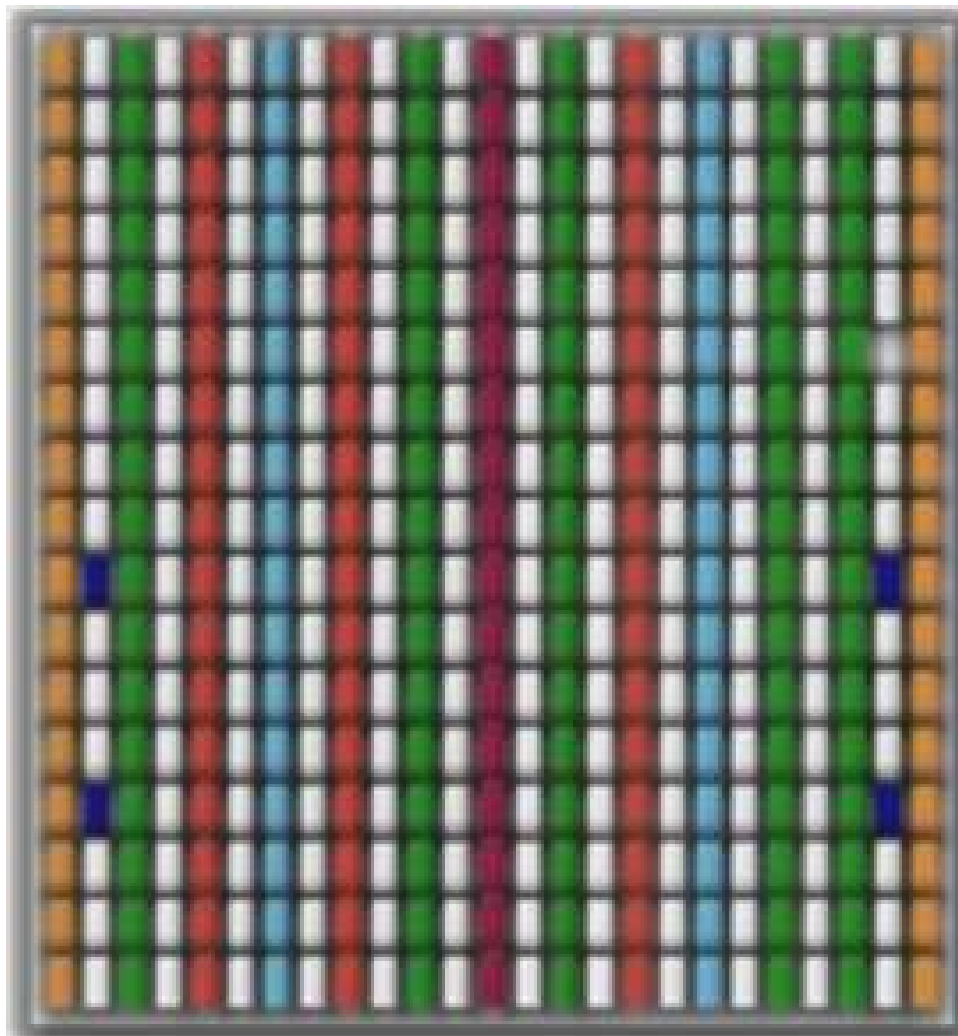
- zapis podczas konfiguracji i odczyt podczas weryfikacji
- podczas normalnej pracy tranzystor wyłączony
- jeden bit danych - steruje jednym punktem konfiguracji
- niewrażliwa na duże dawki promieniowania alfa








Xilinx Artix-7 Parametry podstawowe



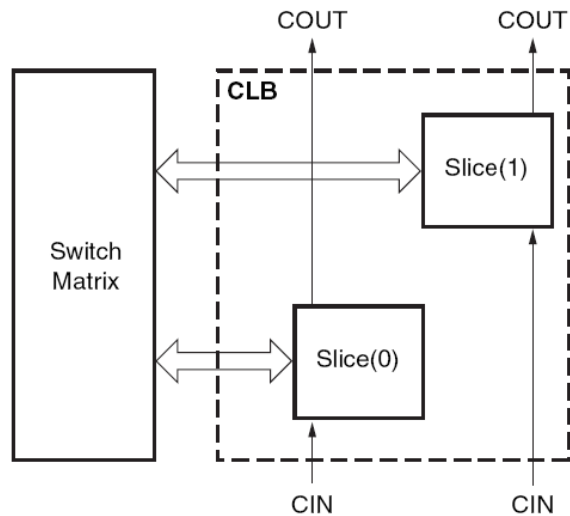
- technologia 28 nm
- struktura gruboziarnista
- 13k – 215k komórek logicznych
- 16k – 270k przerzutników
- 1412 MHz *max toggle frequency*
- zegary – CMTs: 3...10
- pamięć użytkowa Select RAM+
 - rozproszona: do 2888 Kb
 - blokowa: do 13140 Kb
 - zewnętrzna
- 25b × 18b DSP48 MAC: 40...740
- PCIe ..×4 ..Gen2, GTP: 2...16, XADC
- User I/Os
 - pins: 150...500
 - banki: 3...10
- pamięć konfiguracji SRAM
- port JTAG (test + konfiguracja)
- zasilanie:

V_{CCINT} : 0,9...1,0 V	V_{CCBRAM} : 0,95...1,0 V
V_{CCAUX} : 1,8 V	V_{CCO} : 1,2...3,3V
$V_{MGTAVCC}$: 1,0 V	V_{CCADC} : 1,8 V



-  **High Performance Serial I/O Connectivity** MGT
-  **High Performance Parallel I/O Connectivity** SelectIO
-  **Logic fabric** LUT-6 CLB
-  **On-Chip Memory** 36/18Kb BlockRAM
-  **DSP Engines** LUT-6 CLB
-  **Precise Low Jitter Clocking** MMCM
-  **Enhanced Connectivity** PCIe

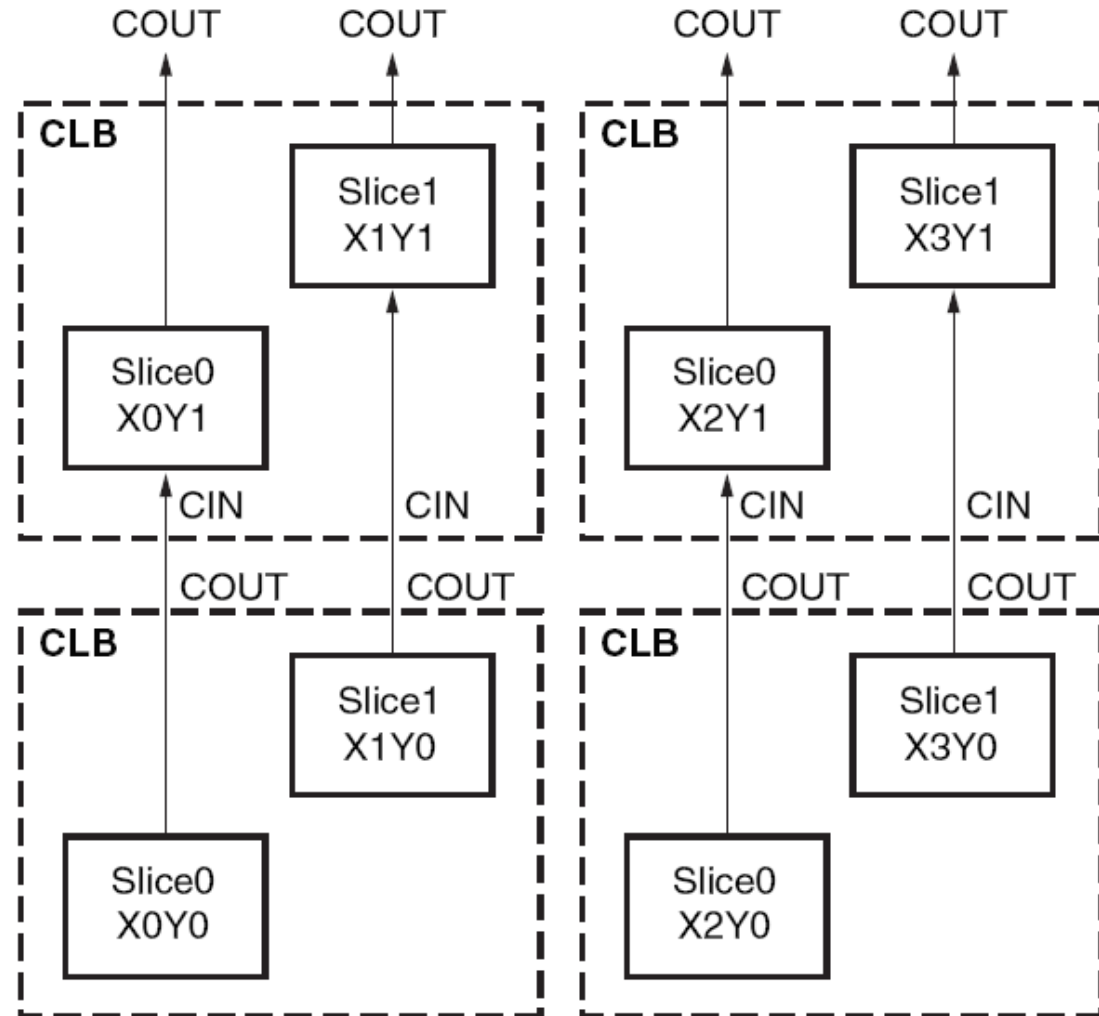
Xilinx Artix-7 Configurable Logic Block

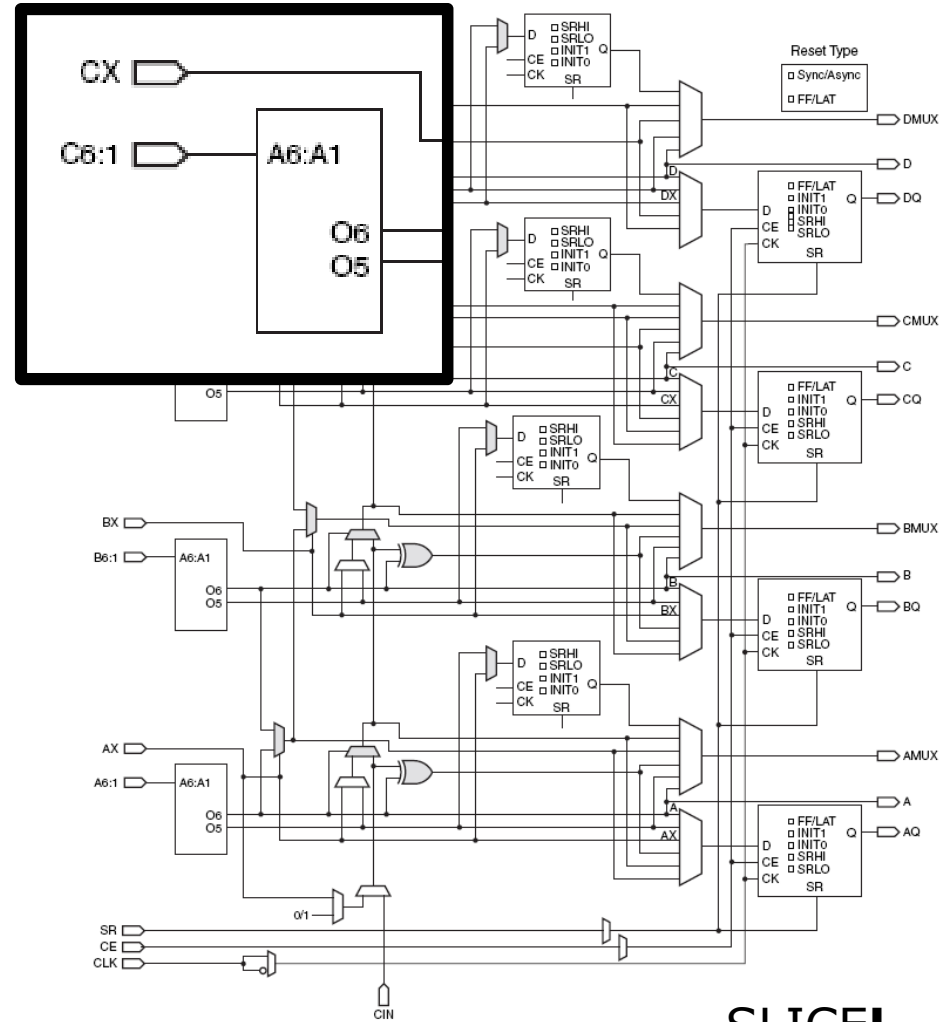
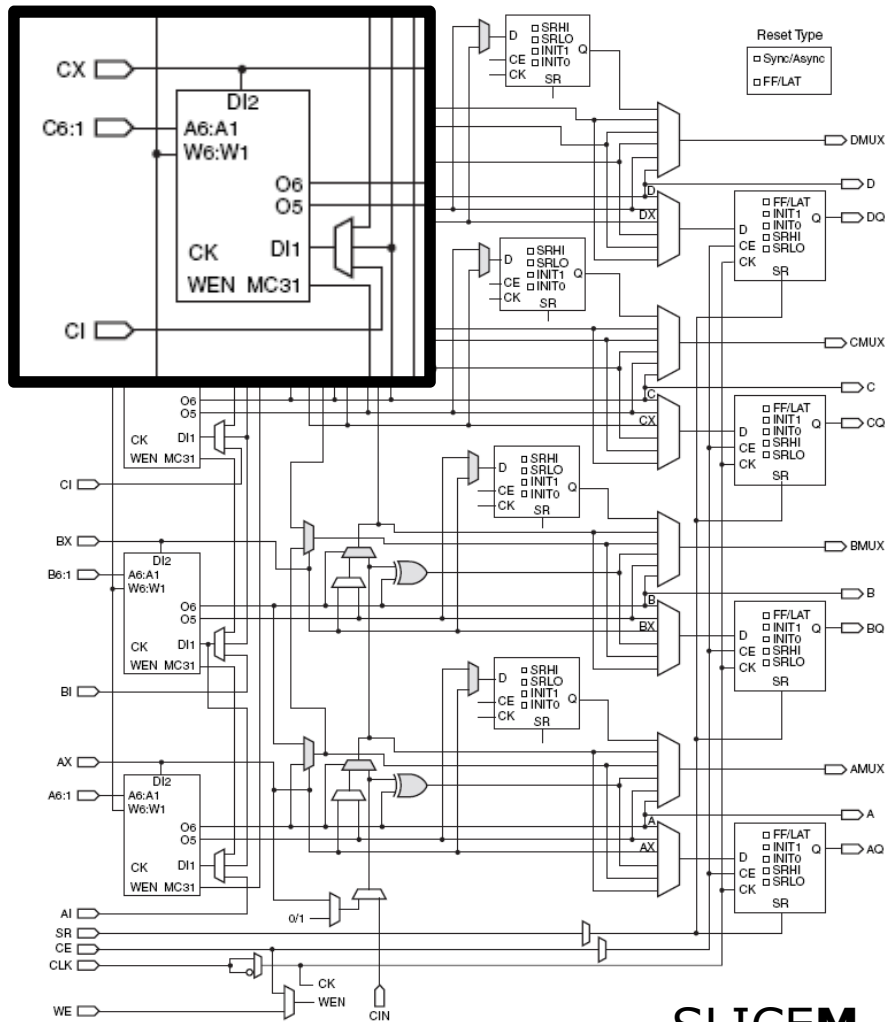


CLB = 2 x LS = 8 x LC

Logic Cell:

- 2 przerzutniki / 1 zatrząsk
- *Clock Enable* ☞
- AP / AC / SS / SR
- jedna 6-we lub dwie 5-we LUT (*Look-Up-Table*)
- *carry logic*

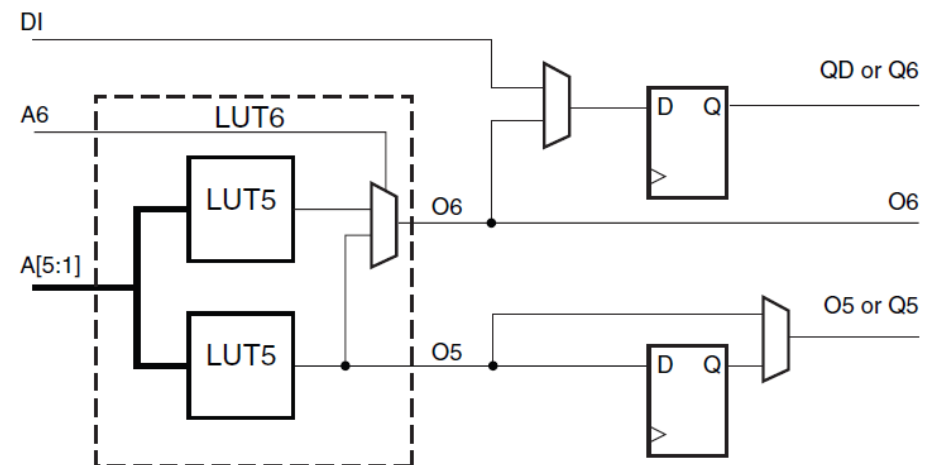




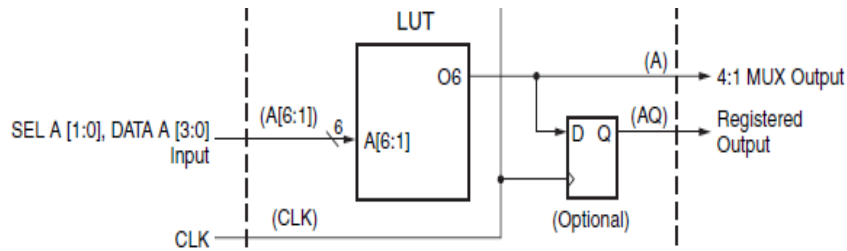
Feature	SLICEL	SLICEM
6-Input LUTs	√	√
8 Flip-flops	√	√
Wide Multiplexers	√	√
Carry Logic	√	√
Distributed RAM		√
Shift Registers		√

LUT6:

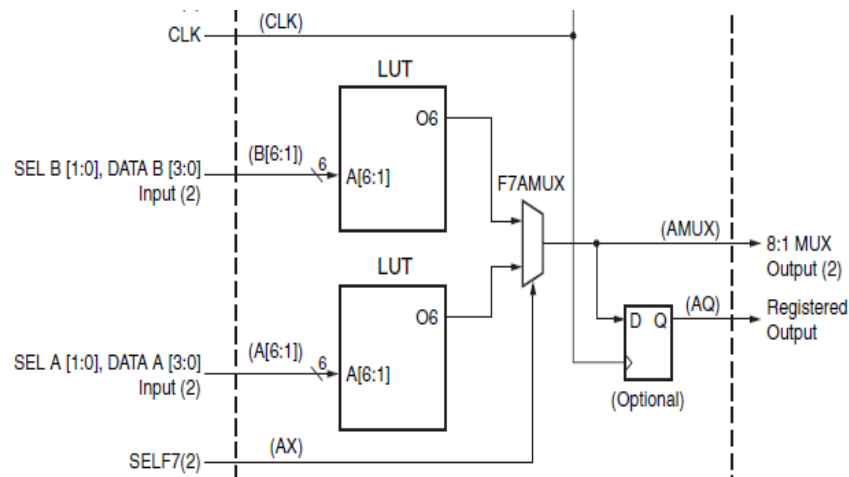
- 6-wejściowy generator funkcji
- SinglePort / DualPort RAM
- 32-stopniowy rejestr przesuwany



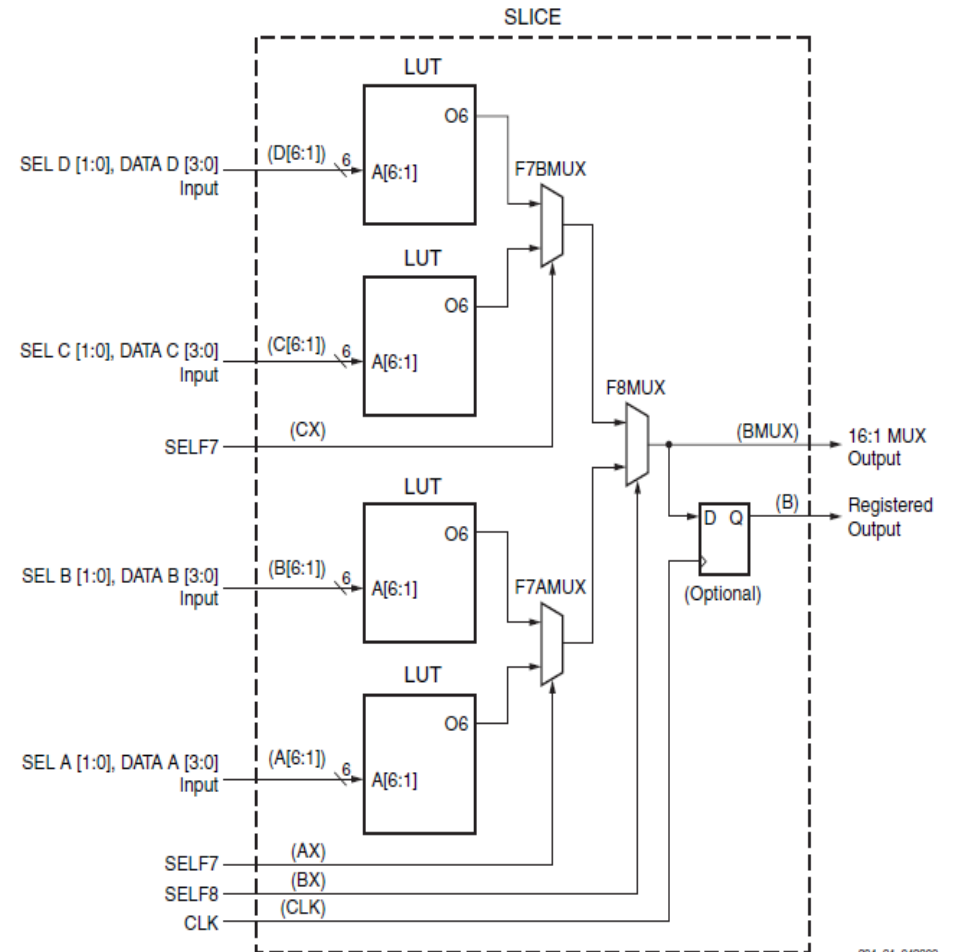
Xilinx Artix-7 Configurable Logic Block: LUT i multipleksery



Mux 2:1 / Fun 6-we

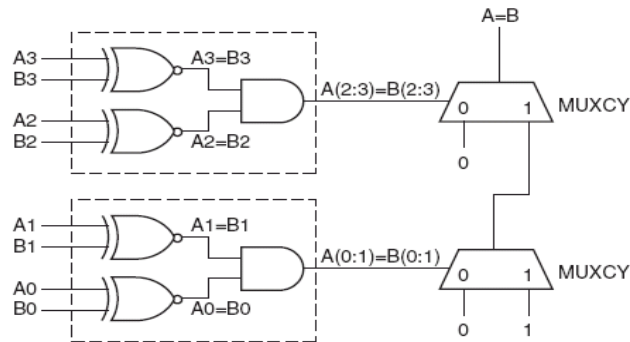


Mux 4:1 / Fun 7-we (do 13-we)

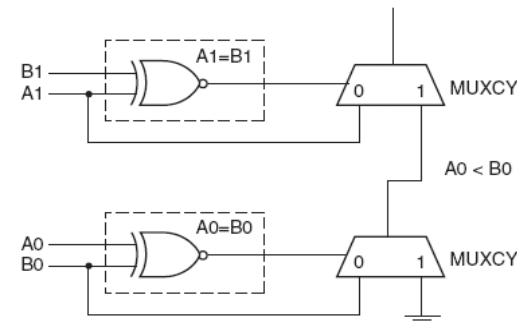


Mux 8:1 / Fun 8-we (do 27-we)

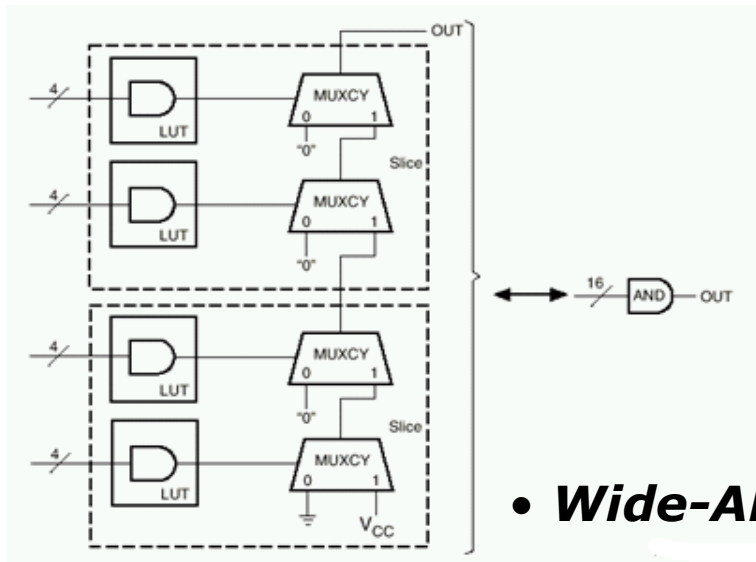
Xilinx Spartan-3 Configurable Logic Block: Carry & Arithmetic



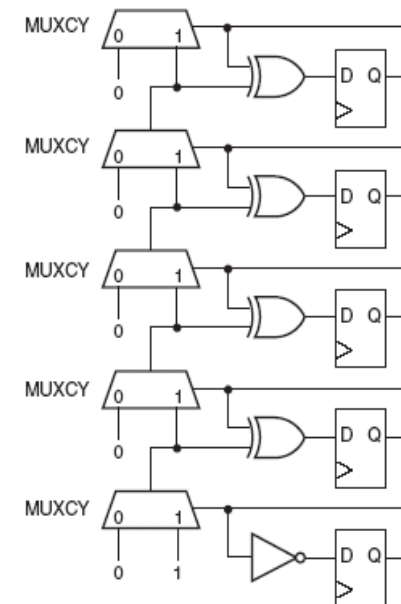
- **Equality Comparator**



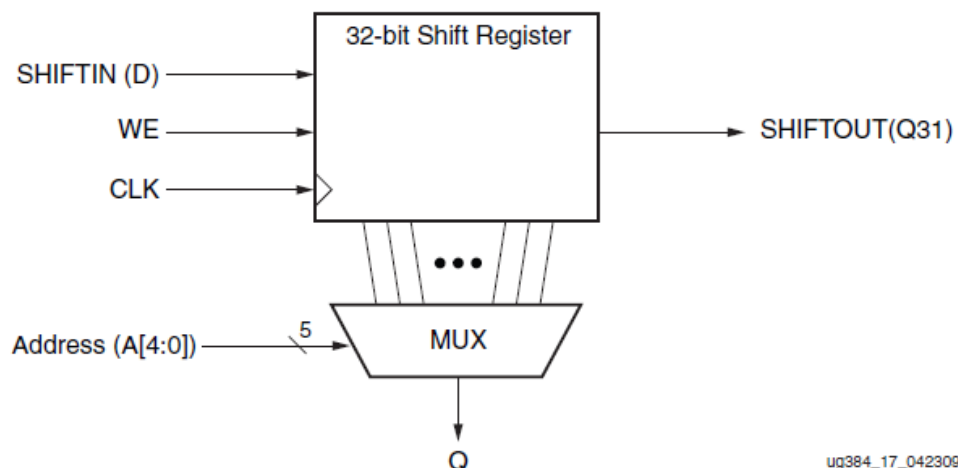
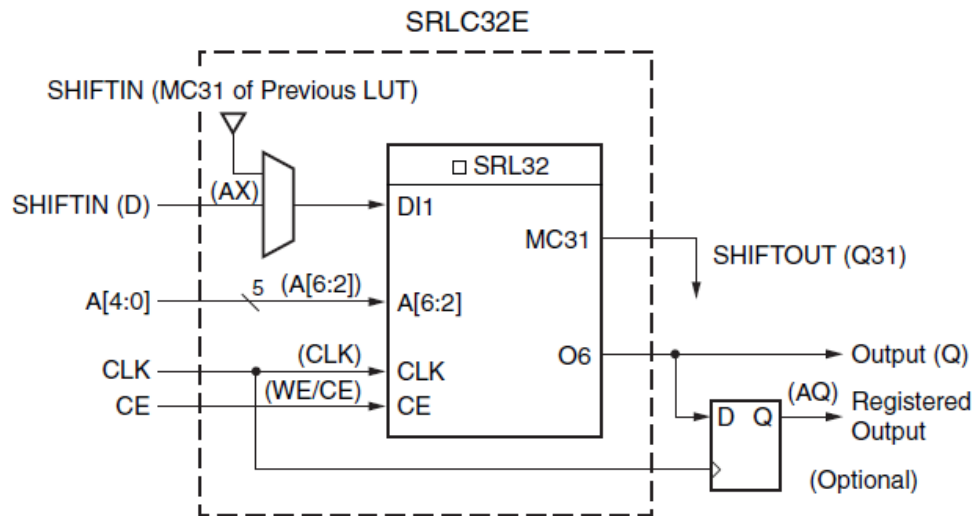
- **Magnitude Comparator**



- **Wide-AND**



- **Licznik**



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Zastosowania:

- długie linie opóźniające
- długie liczniki (także LFSR)
- synchroniczne FIFO
- generatory pseudolosowe

Mutacje:

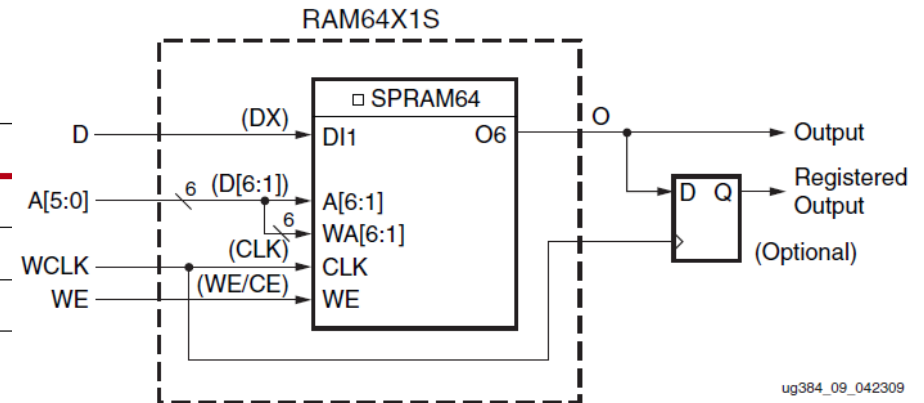
- podwójny 16-bitowy
- kaskada: 64, 96, 128-bit
- dłuższe – połączenia ogólne

Xilinx Artix-7

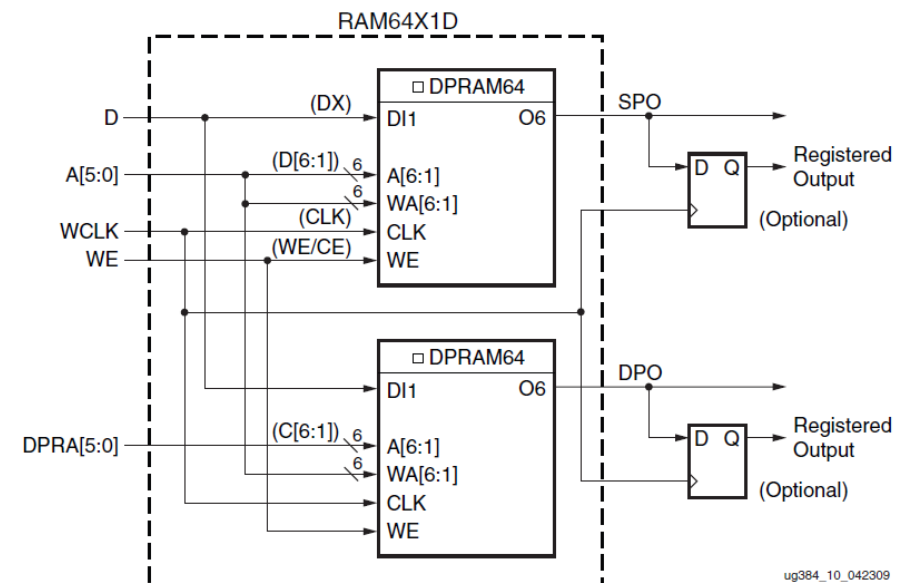
LUT: Distributed RAM

ROM	Number of LUTs
64 x 1	1
128 x 1	2
256 x 1	4

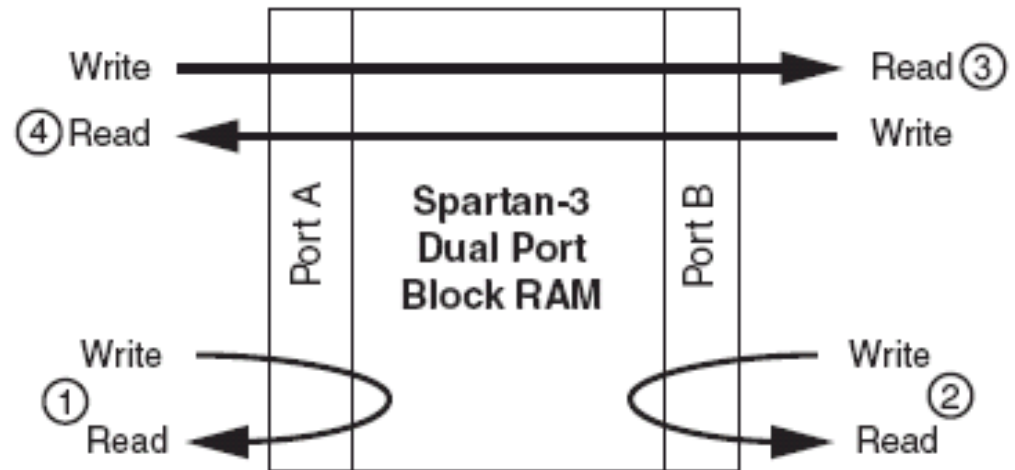
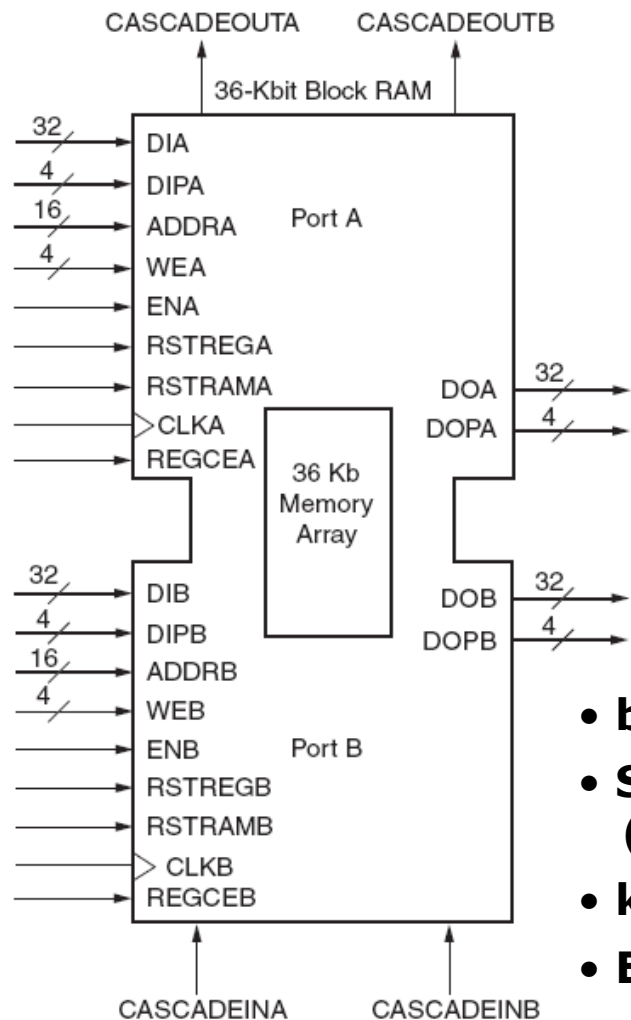
RAM	Description	Primitive	Number of LUTs
32 x 1S	Single port	RAM32X1S	1
32 x 1D	Dual port	RAM32X1D	2
32 x 2Q	Quad port	RAM32M	4
32 x 6SDP	Simple dual port	RAM32M	4
64 x 1S	Single port	RAM64X1S	1
64 x 1D	Dual port	RAM64X1D	2
64 x 1Q	Quad port	RAM64M	4
64 x 3SDP	Simple dual port	RAM64M	4
128 x 1S	Single port	RAM128X1S	2
128 x 1D	Dual port	RAM128X1D	4
256 x 1S	Single port	RAM256X1S	4



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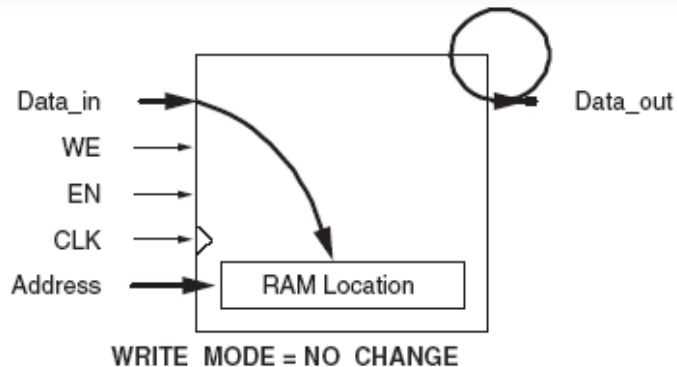
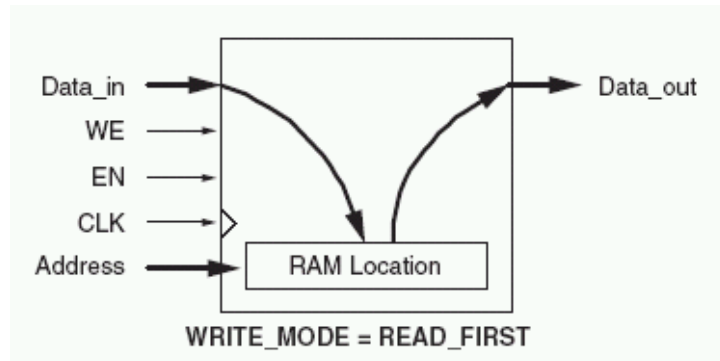
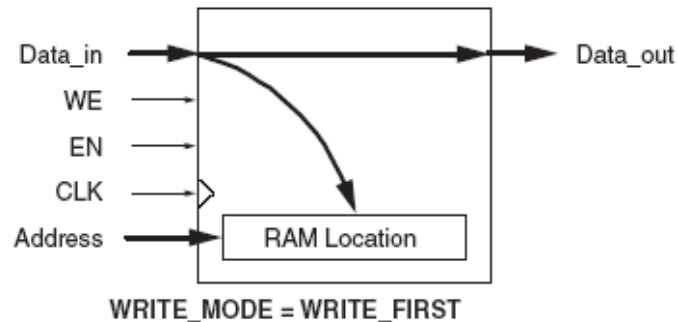


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- blok 36Kb = 2 bloki 18Kb
- Single-Port, Dual-Port (Simple/True Mode)
- kaskadowanie
- ECC

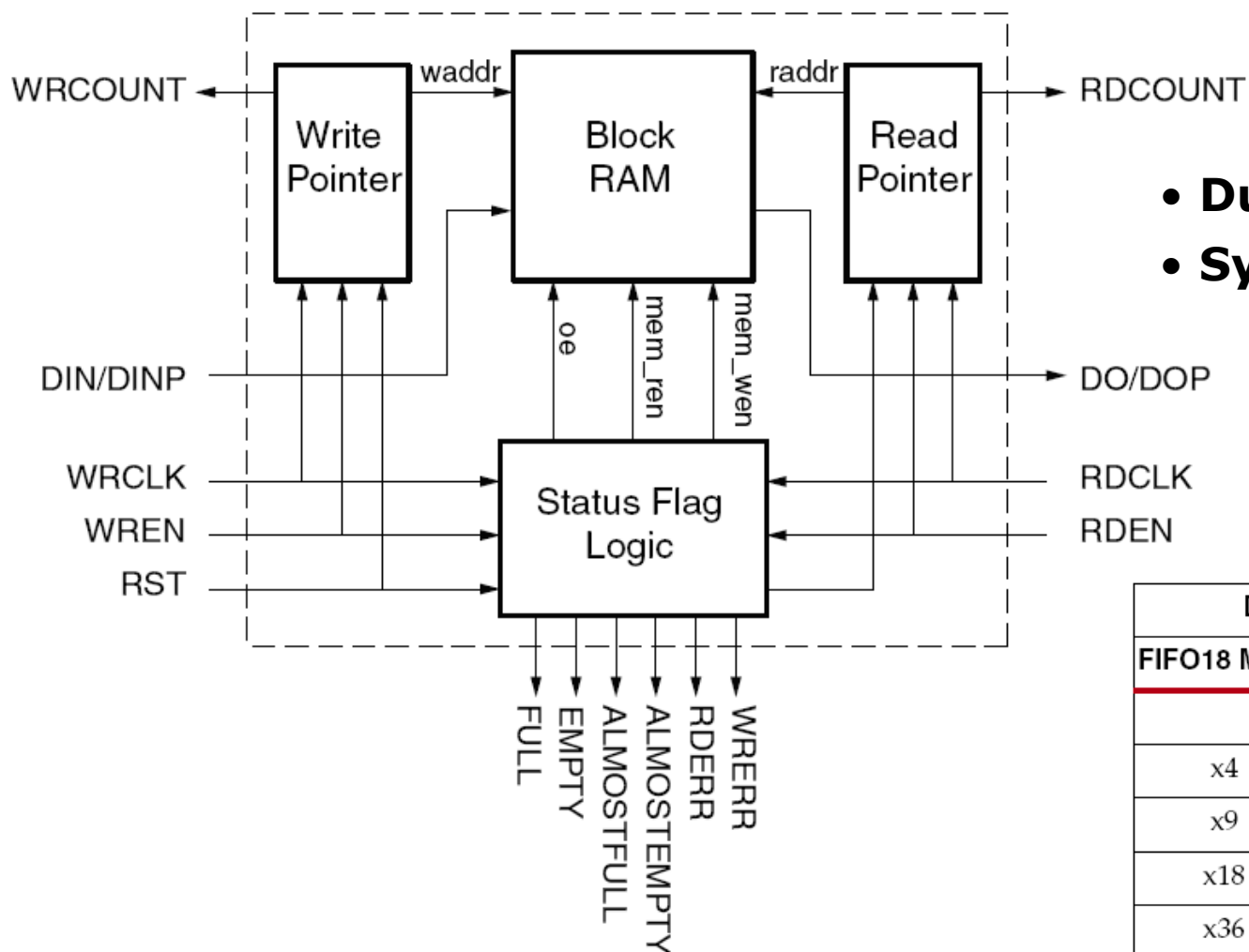
- 64K × 1 (cascaded)
- 32K × 1
- 16K × 2
- 8K × 4
- 4K × 9 (parity)
- 2K × 18 (parity)
- 1K × 36 (parity)
- 512 × 72 (parity, simple)



Zastosowania:

- duże pamięci (łączenie)
- pamięci ROM
- rejestry FIFO
- pamięć programu dla μP
- bufory kołowe
- linie opóźniające
- złożone automaty
- złożone funkcje logiczne
- szybkie, długie liczniki
- pamięci CAM
- pamięci 4-portowe
- tablice funkcji (DDS)

Xilinx Artix-7 Block RAM FIFO

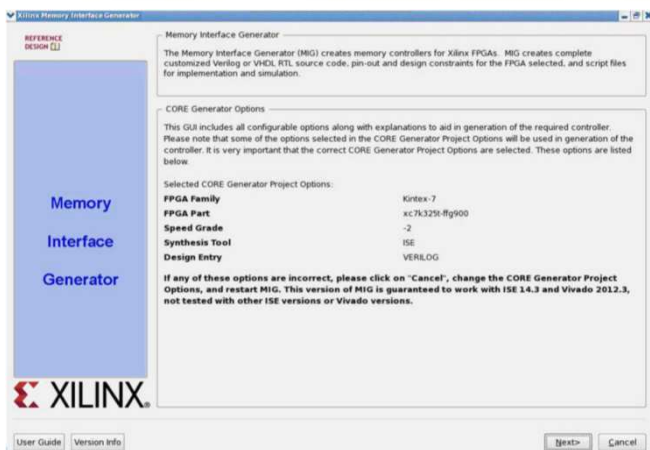


- **Dual-Clock FIFO**
- **Synchronous FIFO**

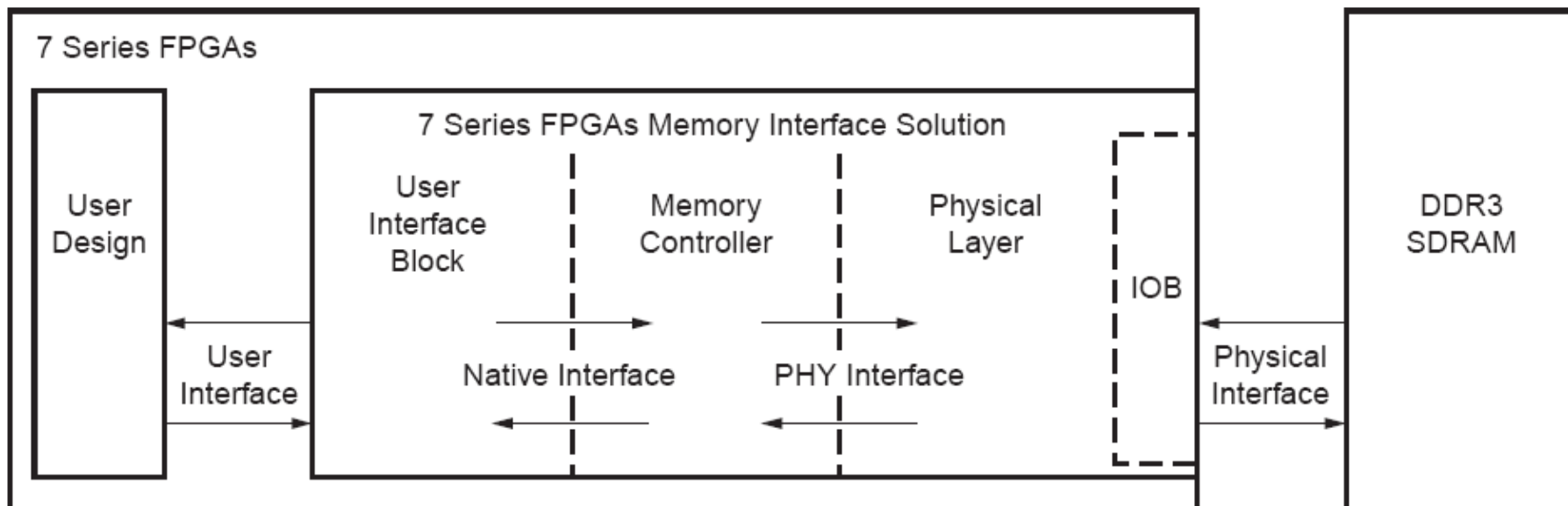
Data Width		Block RAM
FIFO18 Mode	FIFO36 Mode	
	x4	8192
x4	x9	4096
x9	x18	2048
x18	x36	1024
x36	x72	512

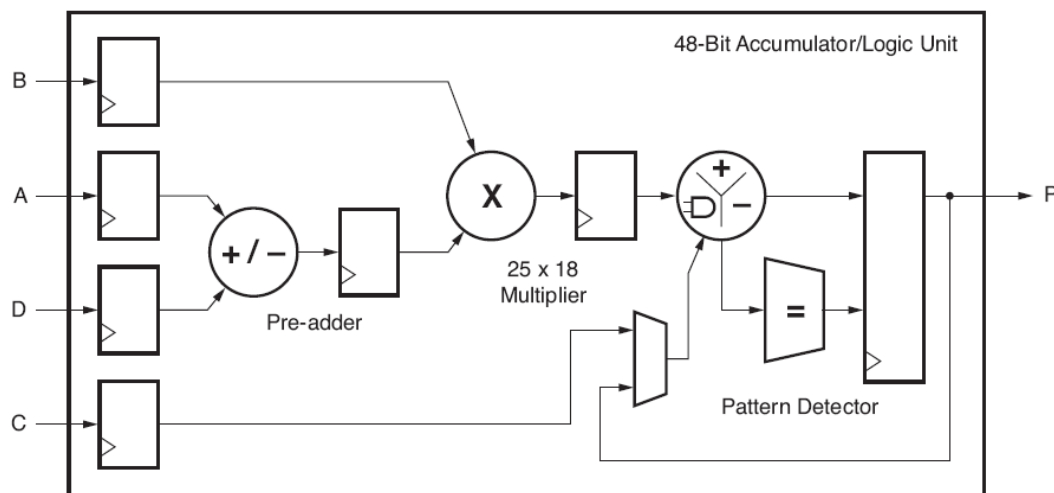


Xilinx Artix-7 Memory Interface Solution



- **DDR3 i DDR2**
- **QDDR II+ SRAM**
- **RLDRAM II / III**
- **do 72 bitów szerokości**
- **1...4Gb**
- **interfejs 8/16-bit**
- **zegar do >1 GHz**

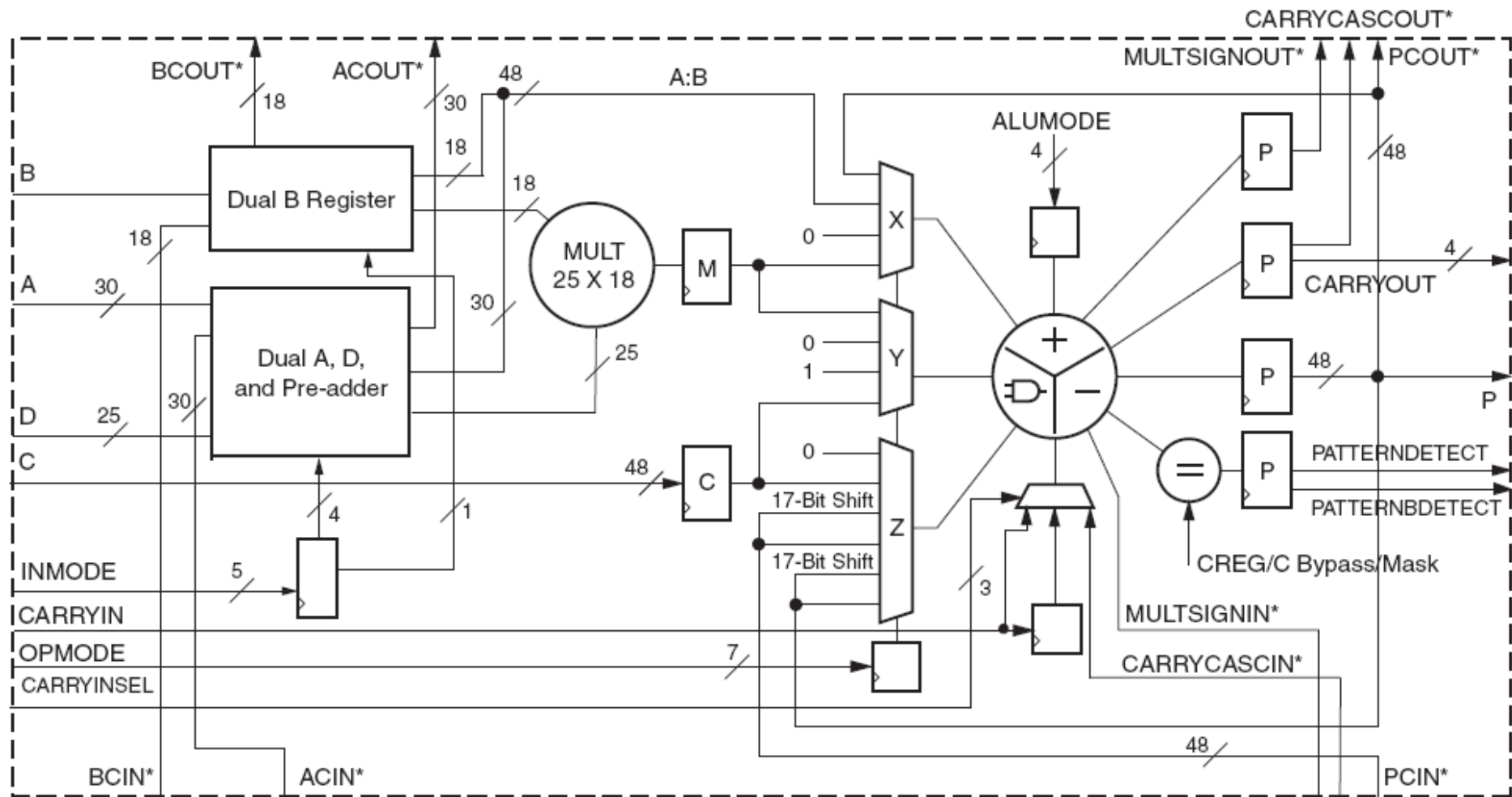




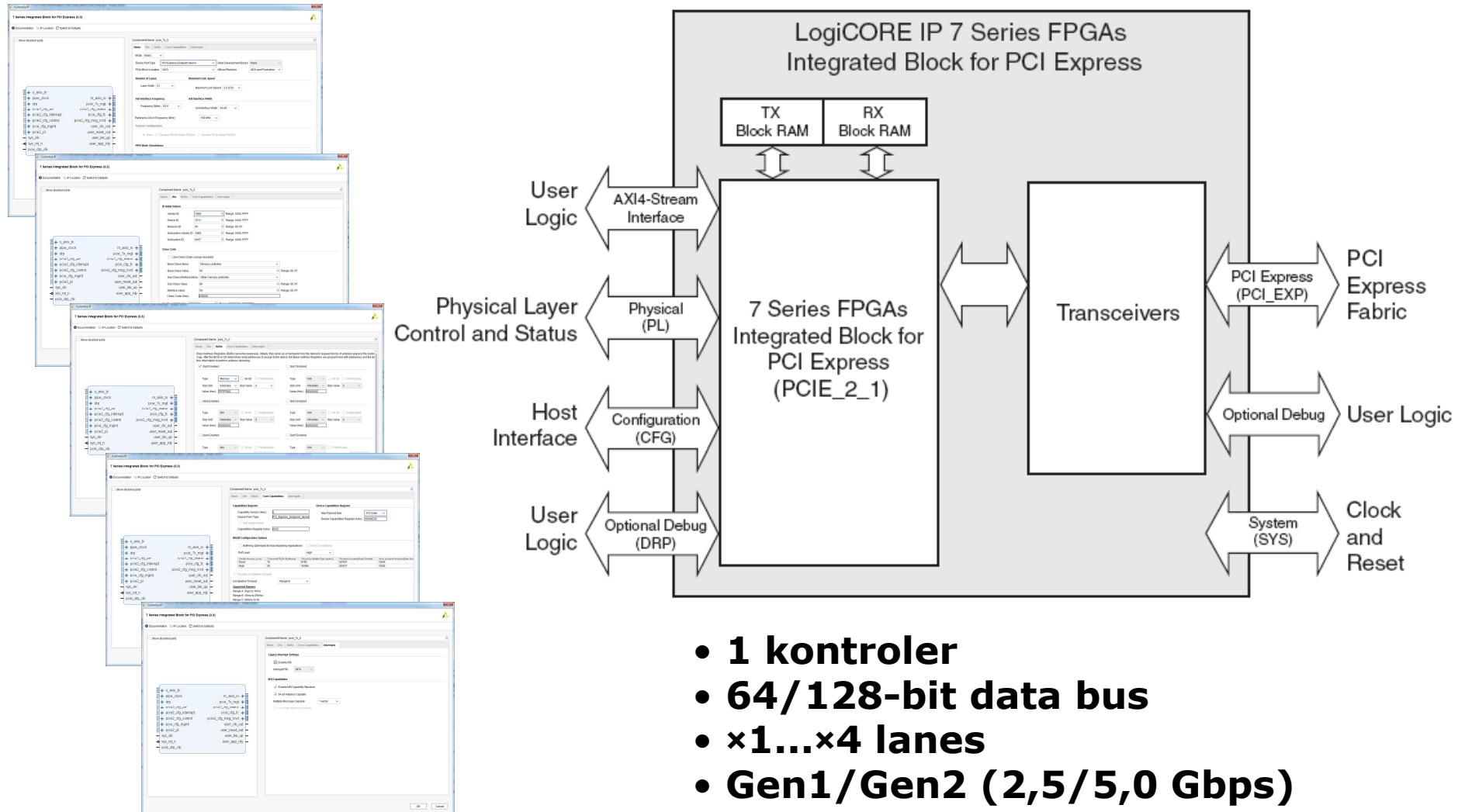
- mnożarka $25b \times 18b$
- akumulator 48b
- preadder
- generator funkcji logicznych
- mnożenie w kodzie U2
- opcjonalne rejestry
- łączenie w większe
- podział na mniejsze
- *pattern detector*

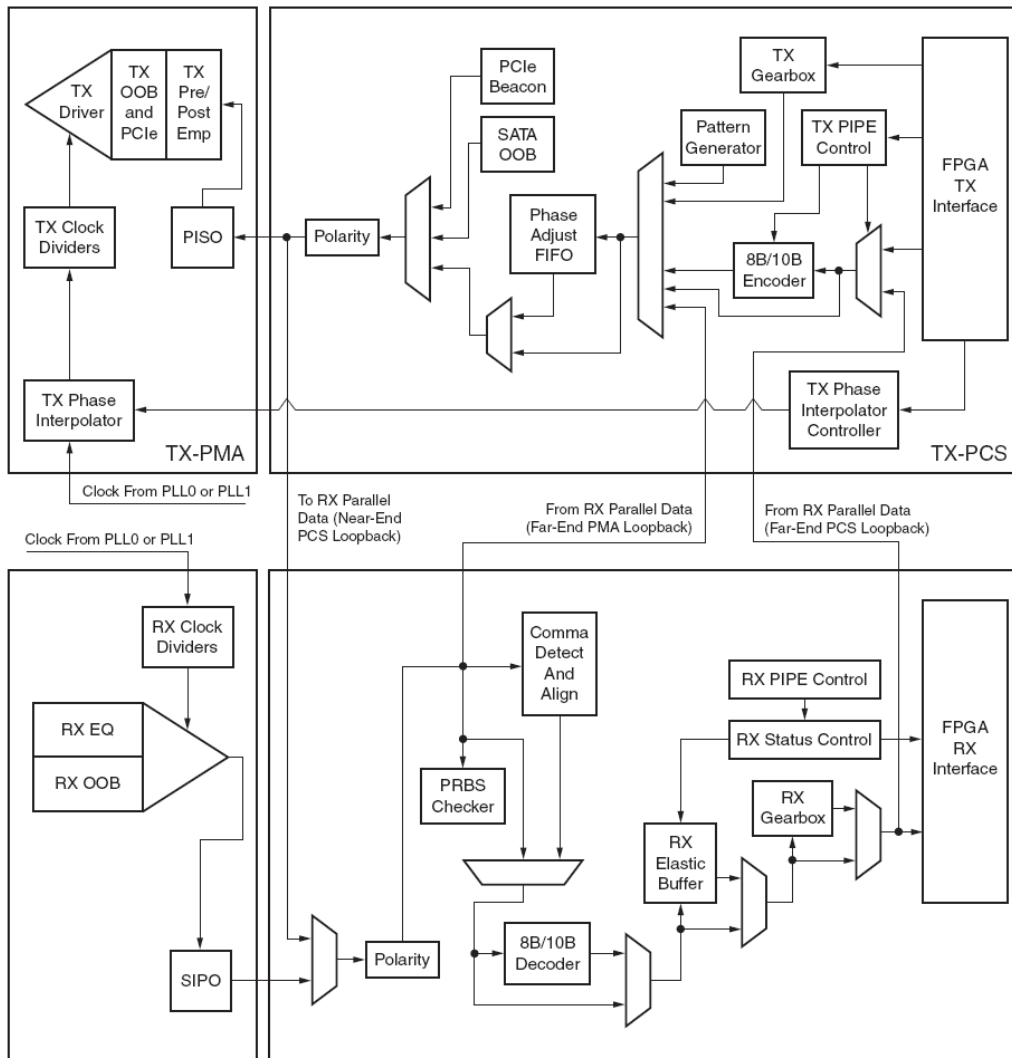
Zastosowania:

- mnożenie
- przesuwanie
- funkcje logiczne
- obliczanie modułu
- generowanie wartości U2
- mnożenie zespolone
- mnożenie macierzy (z podziałem czasu)
- mnożenie zmiennoprzecinkowe

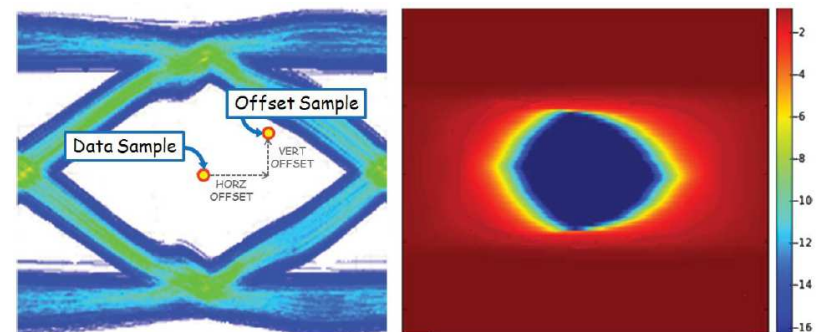


Xilinx Artix-7 PCIe Integrated Endpoint Block



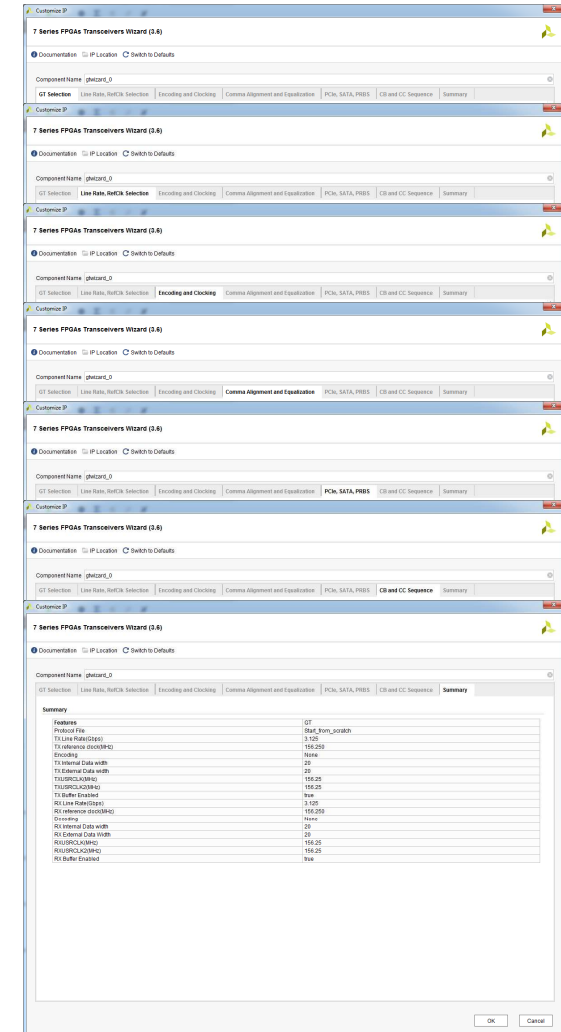
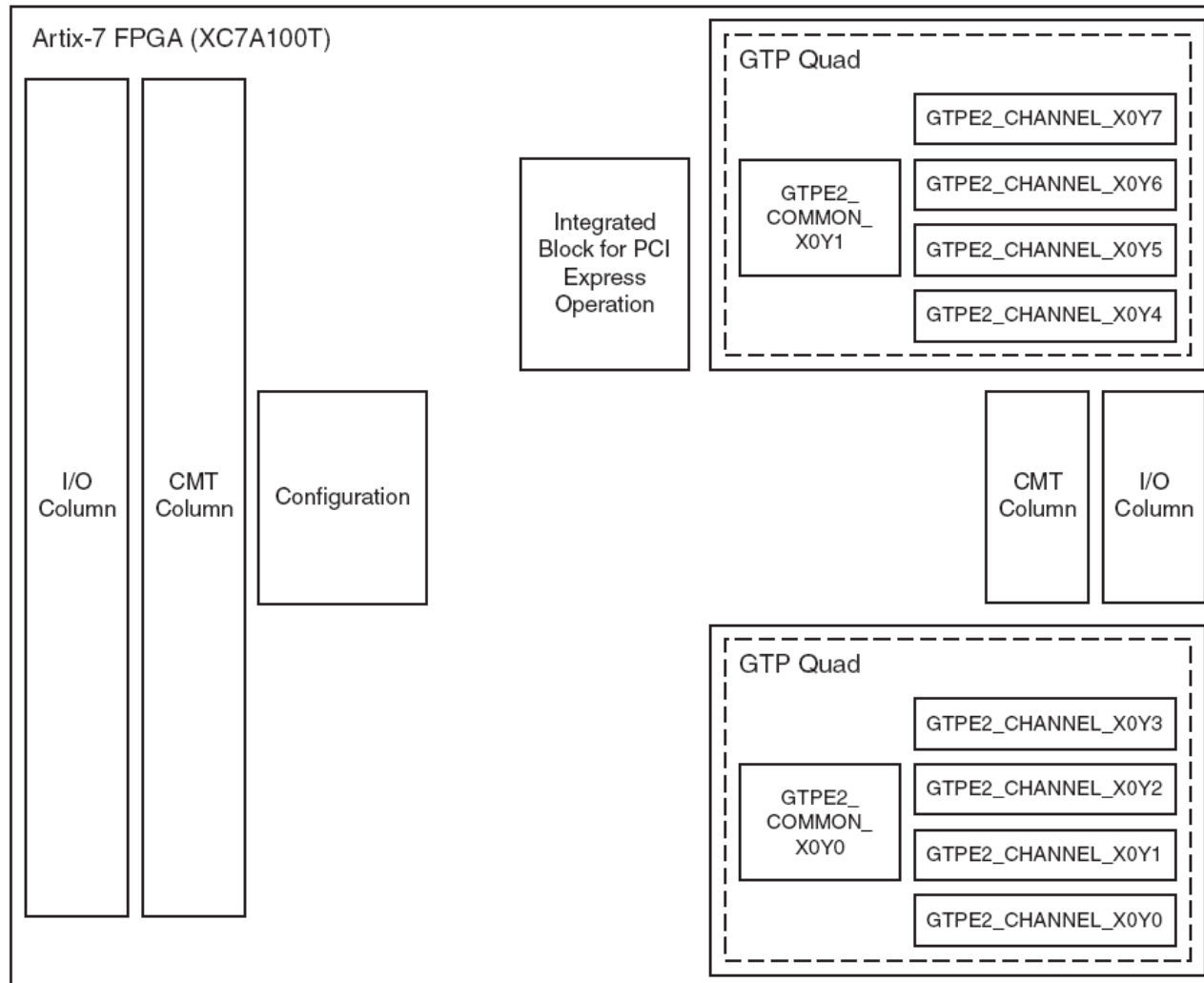


- 2..16 transceiverów
- lane rate range:
0.5...6.6 Gbps
- 8b/10b, gearbox
- suport:
 - PCIe
 - SATA
 - 10GbE XAUI
 - SDI
 - ...
- PRBS, h&v eye-scan

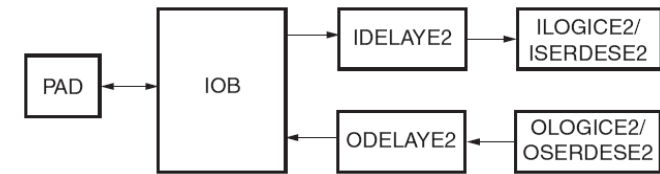
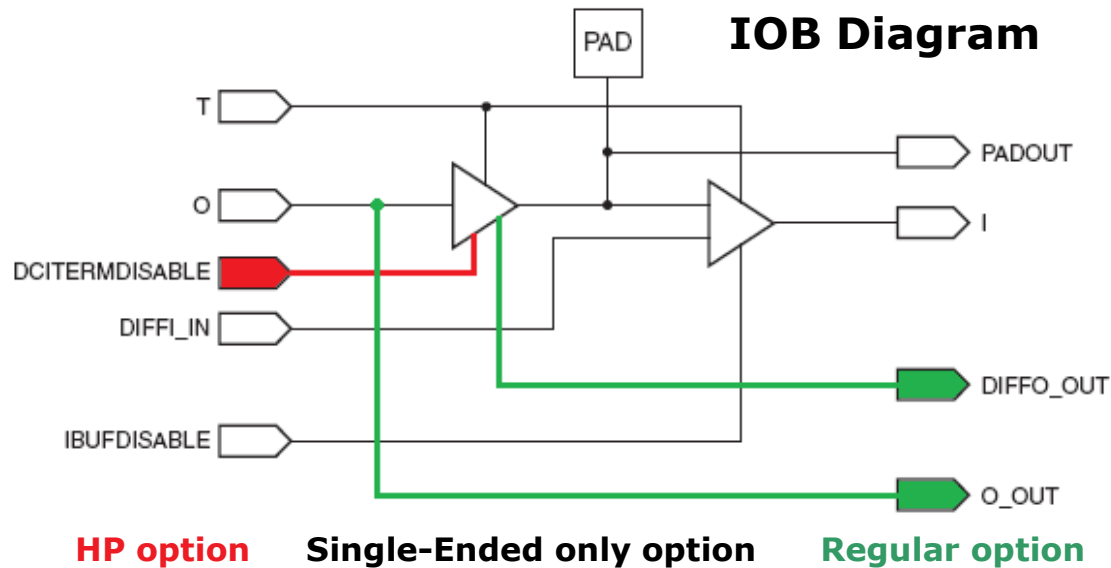




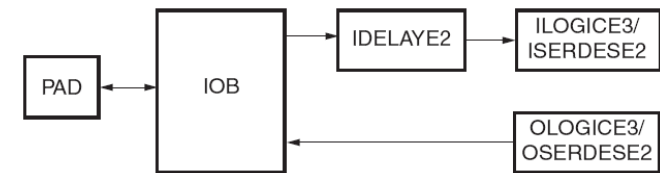
Xilinx Artix-7 GTP Transceivers



Xilinx Artix-7 Input / Output Tiles: HR/HP




7 Series FPGA HP Bank I/O Tile



7 Series FPGA HR Bank I/O Tile

Programowalne:

- pull-up / pull-down
- weak-keeper 
- DCI (Digital Controlled Impedance)
- Output Drive Strength (2...24mA)

Unipolarne:

LVCMOS, LVTTTL, HSTL, PCI, SSTL

Różnicowe:

LVDS, MiniLVDS, RSDS, PPDS, BLVDS, diff HSTL & SSTL

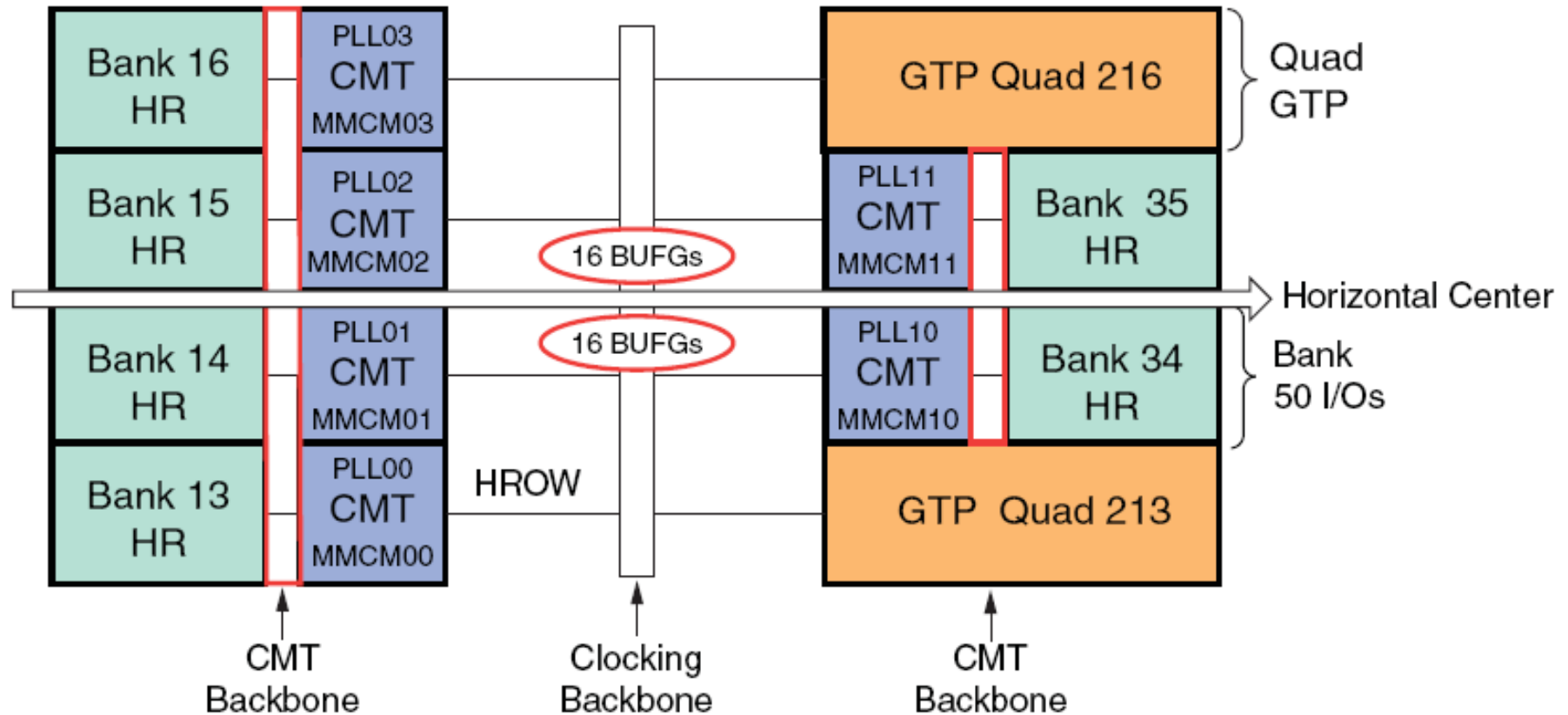
Xilinx Artix-7 SelectIO: XC7A100T-CSG324

Left I/O
Column
Banks

CSG324 Package

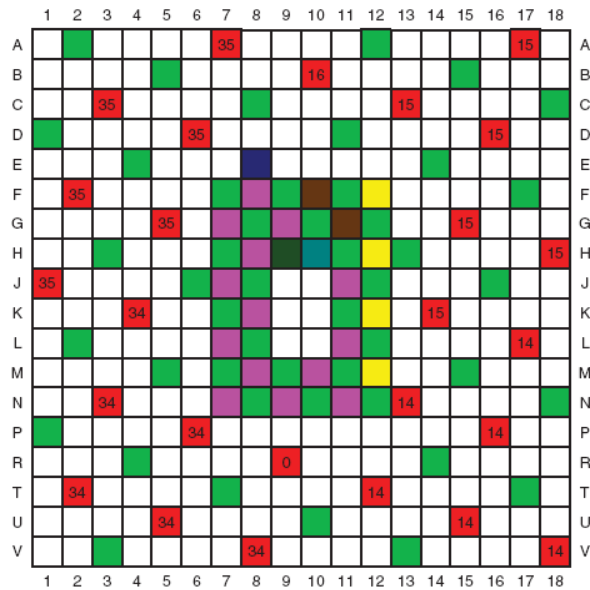
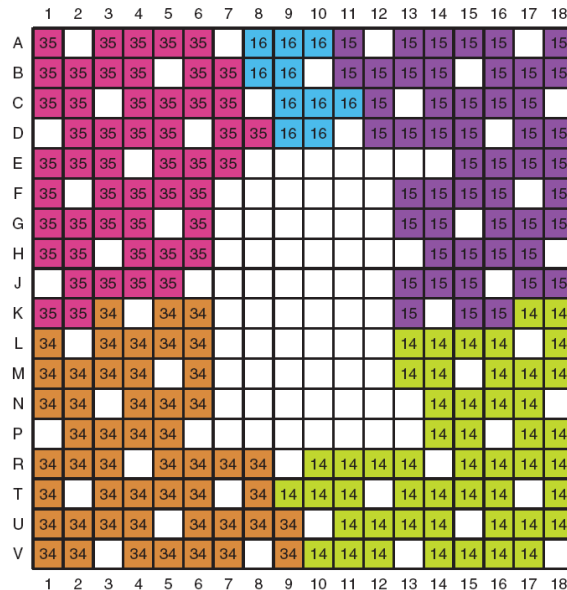
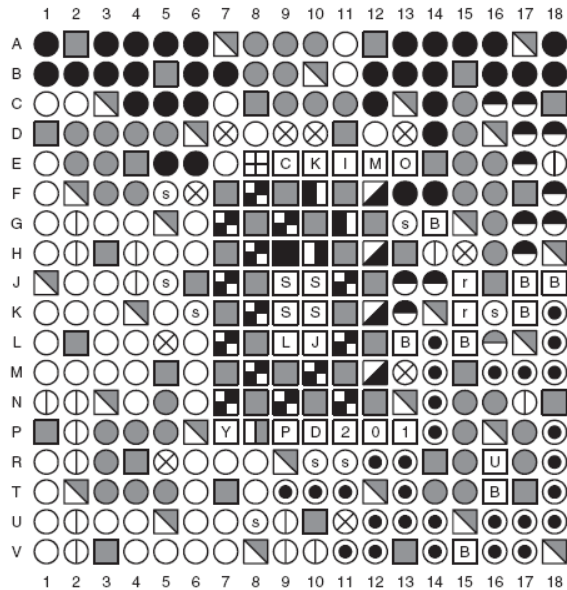
- HR I/O bank 13 is not bonded out.
- HR I/O bank 16 is partially bonded out.
- The GTP Quads 213 and 216 are not bonded out.

Right I/O
Column
Banks





Xilinx Artix-7 XC7A100T-CSG324 Package Pins

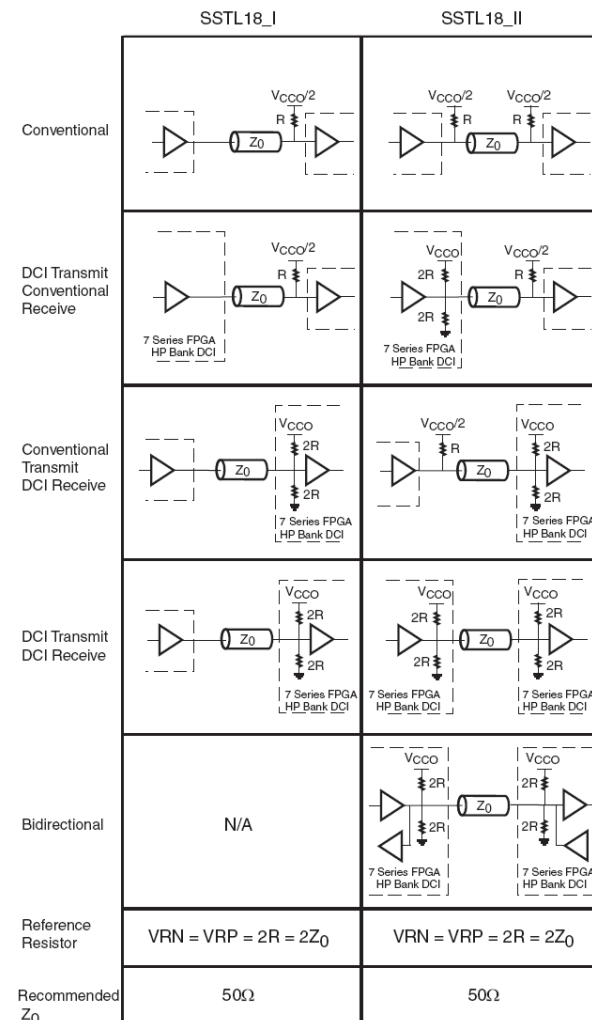


User I/O Pins	Dedicated Pins		Other Pins
<ul style="list-style-type: none"> ○ IO_LXXY_# ○ IO_XX_# 	<ul style="list-style-type: none"> C CCLK_0 I CFGBVS_0 D DONE_0 J DXP_0 L DXN_0 ■ GNDADC_0 Y INIT_B_0 0 M0_0 1 M1_0 2 M2_0 P PROGRAM_B_0 K TCK_0 I TDL_0 O TDO_0 M TMS_0 ■ VCCADC_0 ■ VCCBATT_0 	<ul style="list-style-type: none"> S VP_0 S VN_0 S VREFP_0 S VREFN_0 	<ul style="list-style-type: none"> ■ GND ■ VCCAUX_IO_G# ■ VCCAUX ■ VCCINT ■ VCCO_# ■ VCCBRAM n NC
Multi-Function Pins			
<ul style="list-style-type: none"> B ADV_B B FCS_B B FOE_B B MOSI B FWE_B B DOUT_CSO_B B CSI_B B PUDC_B U RDWR_B r RS0-RS1 ● AD0P/AD0N-AD15P/AD15N ○ EMCCLK 	<ul style="list-style-type: none"> ⊕ VRN ⊖ VRP ⊗ VREF ● D00-D31 ● A00-A28 ○ DQS ● MRCC ● SRCC 		

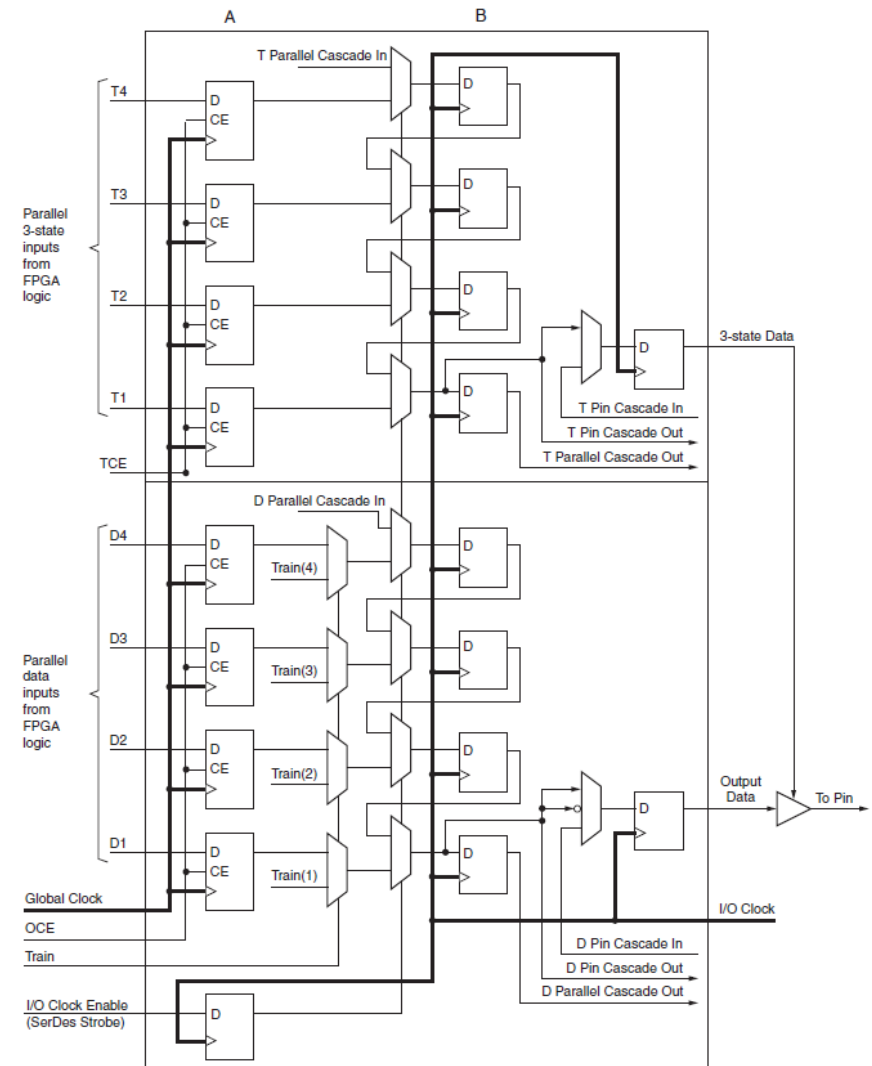
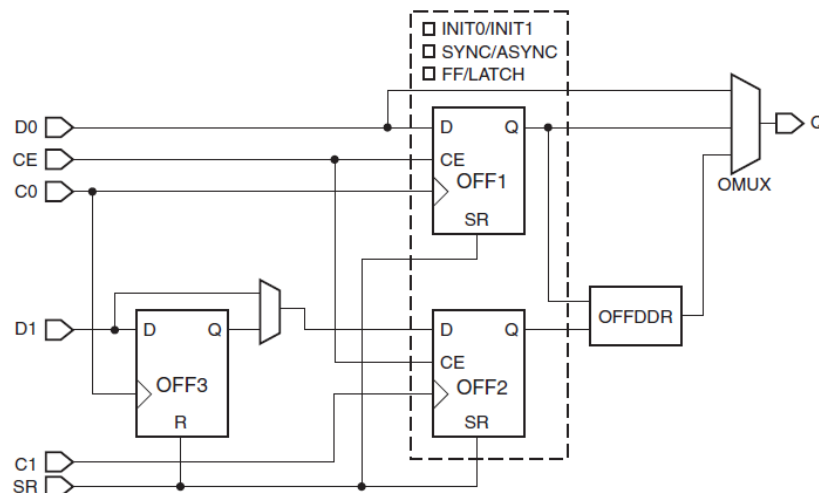
Power Pins	
#	VCCO_#
■	VCCINT
■	VCCAUX
#	VCCAUX_IO_G#
■	VCCBRAM
■	VCCBATT_0
■	VCCADC_0
■	GNDADC_0
■	GND

Xilinx Artix-7 SelectIO: HR/HP features, DCI option

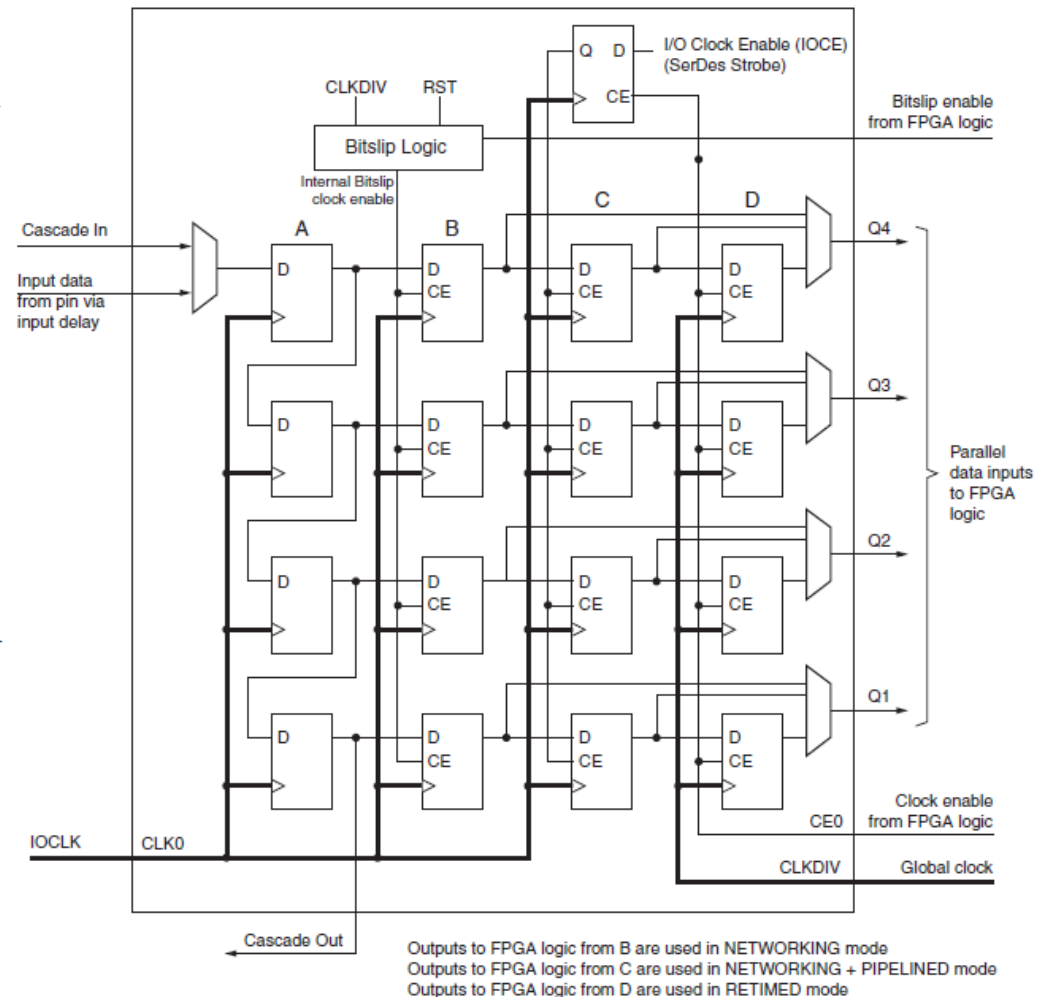
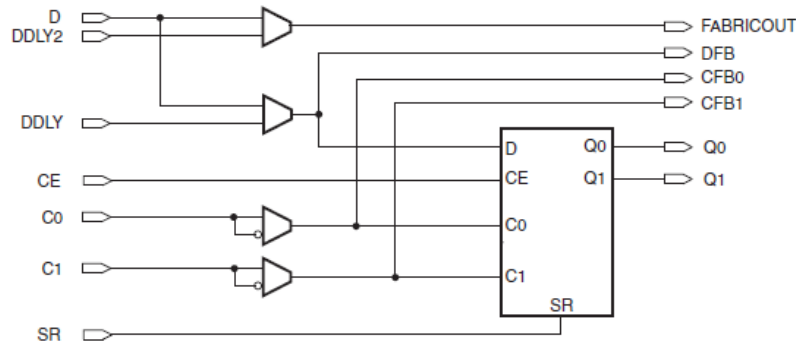
Feature	HP I/O Banks	HR I/O Banks
3.3V I/O standards ⁽¹⁾	N/A	Supported
2.5V I/O standards ⁽¹⁾	N/A	Supported
1.8V I/O standards ⁽¹⁾	Supported	Supported
1.5V I/O standards ⁽¹⁾	Supported	Supported
1.35V I/O standards ⁽¹⁾	Supported	Supported
1.2V I/O standards ⁽¹⁾	Supported	Supported
LVDS signaling	Supported ⁽²⁾	Supported
24 mA drive option for LVCMOS18 and LVTTTL outputs	N/A	Supported
V _{CCAUX_IO} supply rail	Supported	N/A
Digitally-controlled impedance (DCI) and DCI cascading	Supported	N/A
Internal V _{REF}	Supported	Supported
Internal differential termination (DIFF_TERM)	Supported	Supported
IDELAY	Supported	Supported
ODELAY	Supported	N/A
IDELAYCTRL	Supported	Supported
ISERDES	Supported	Supported
OSERDES	Supported	Supported
ZHOLD_DELAY	N/A	Supported

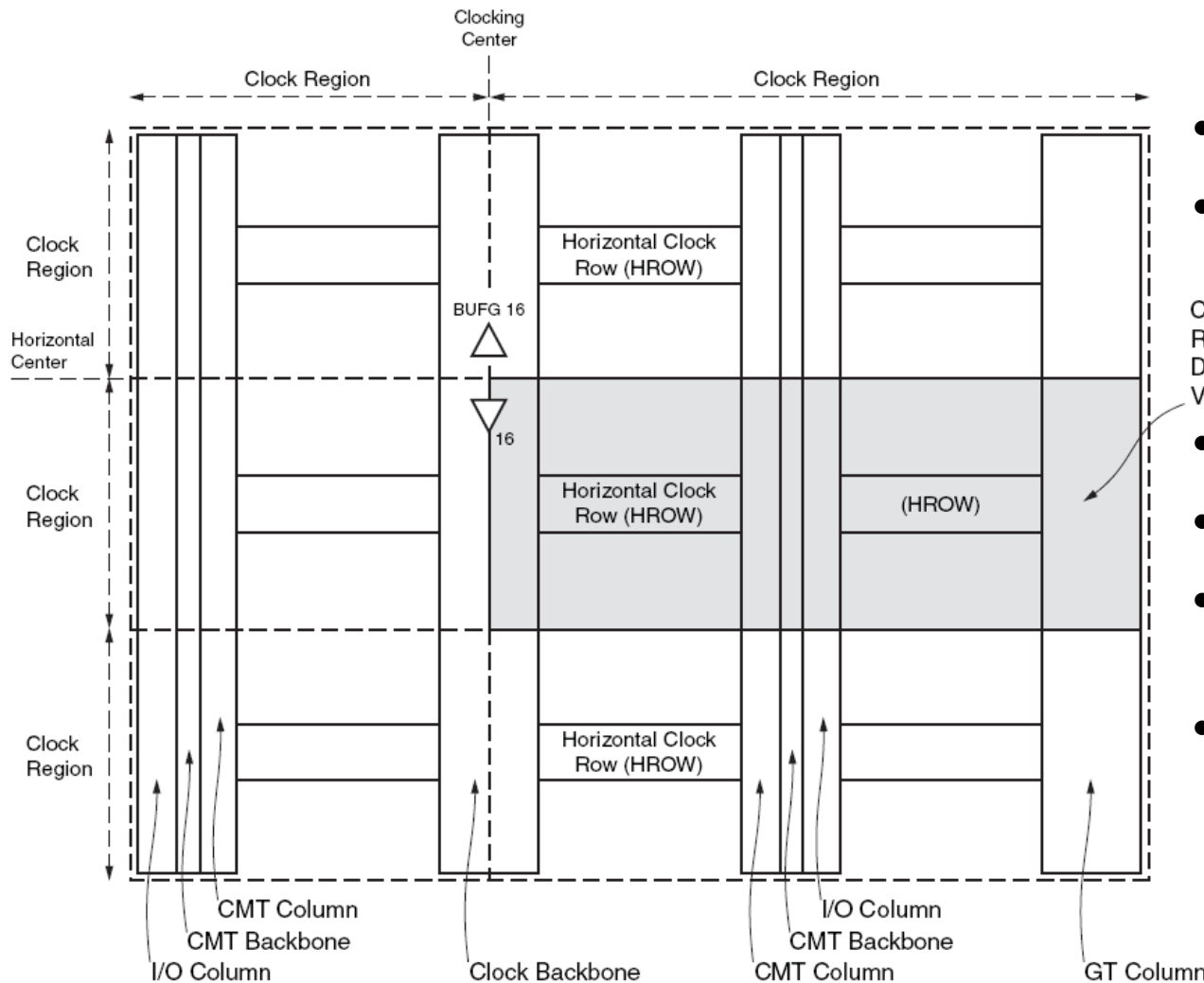


- SDR / DDR
- OFF3 – DDR data alignment
- serializacja: 2,3,4,5,6,7,8 SDR
4,6,8,10,14 DDR
- niezależna ścieżka Tri-State
- training pattern



- SDR FF/LATCH, DDR FF
- serializacja: 2,3,4,5,6,7,8 SDR
4,6,8,10,14 DDR
- bit-slip
- 3 stopnie synchronizacji





- **1...24 Clock Regions**

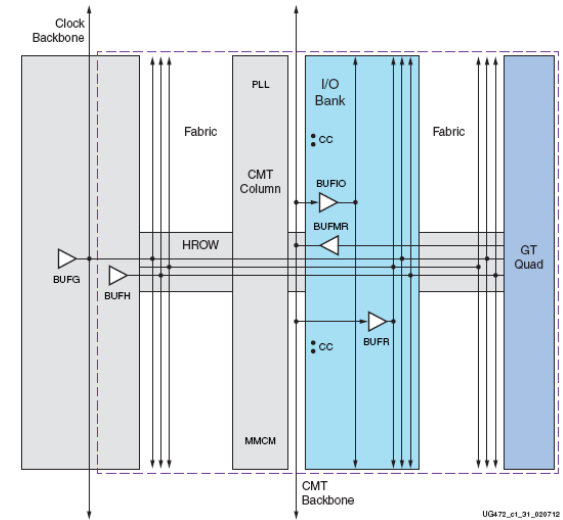
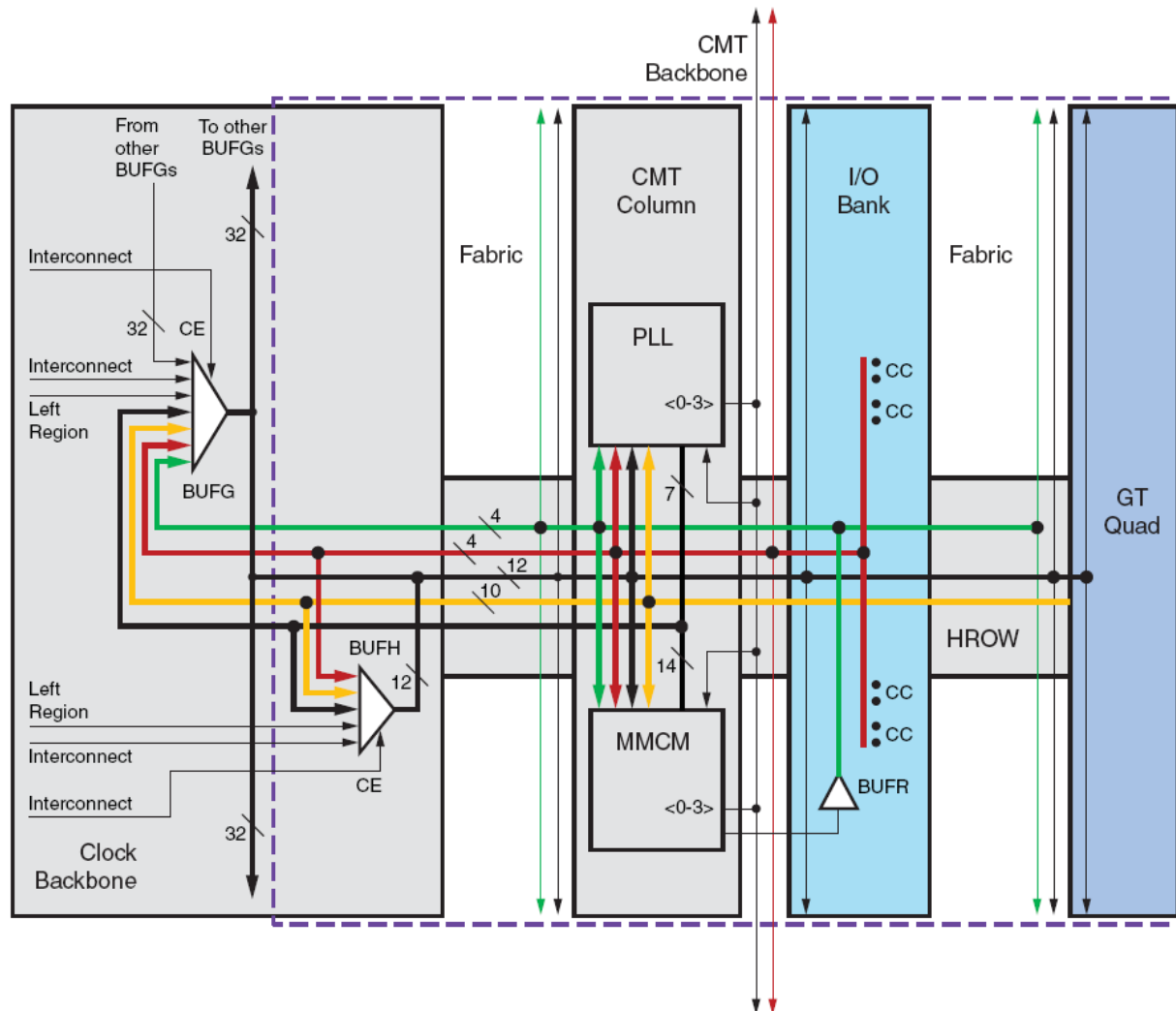
- **CR is 50 CLBs high**

- **HROW in center of CR**

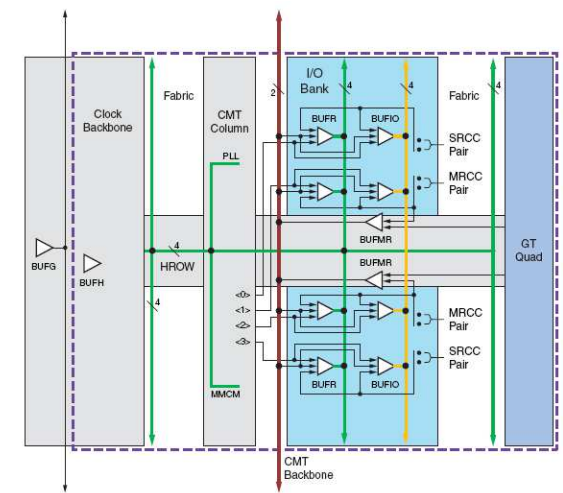
- **SRCC / MRCC pins**

- **Clock Management Tiles**

- **Buffers: BUFIO, BUFR, BUFMR, BUFH, BUFG, BUFGCE, BUFGMUX**



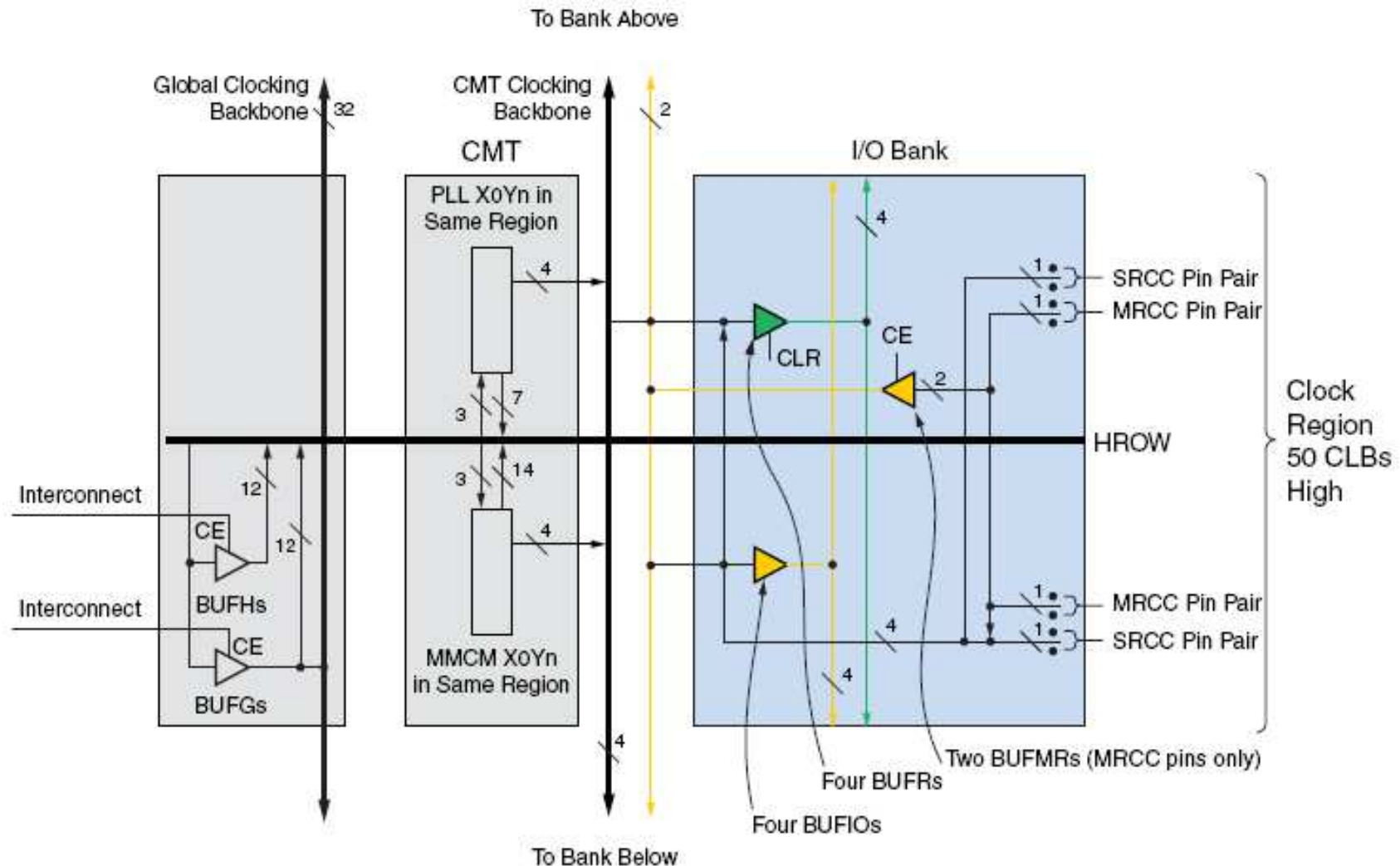
UG472_v1_01_201712



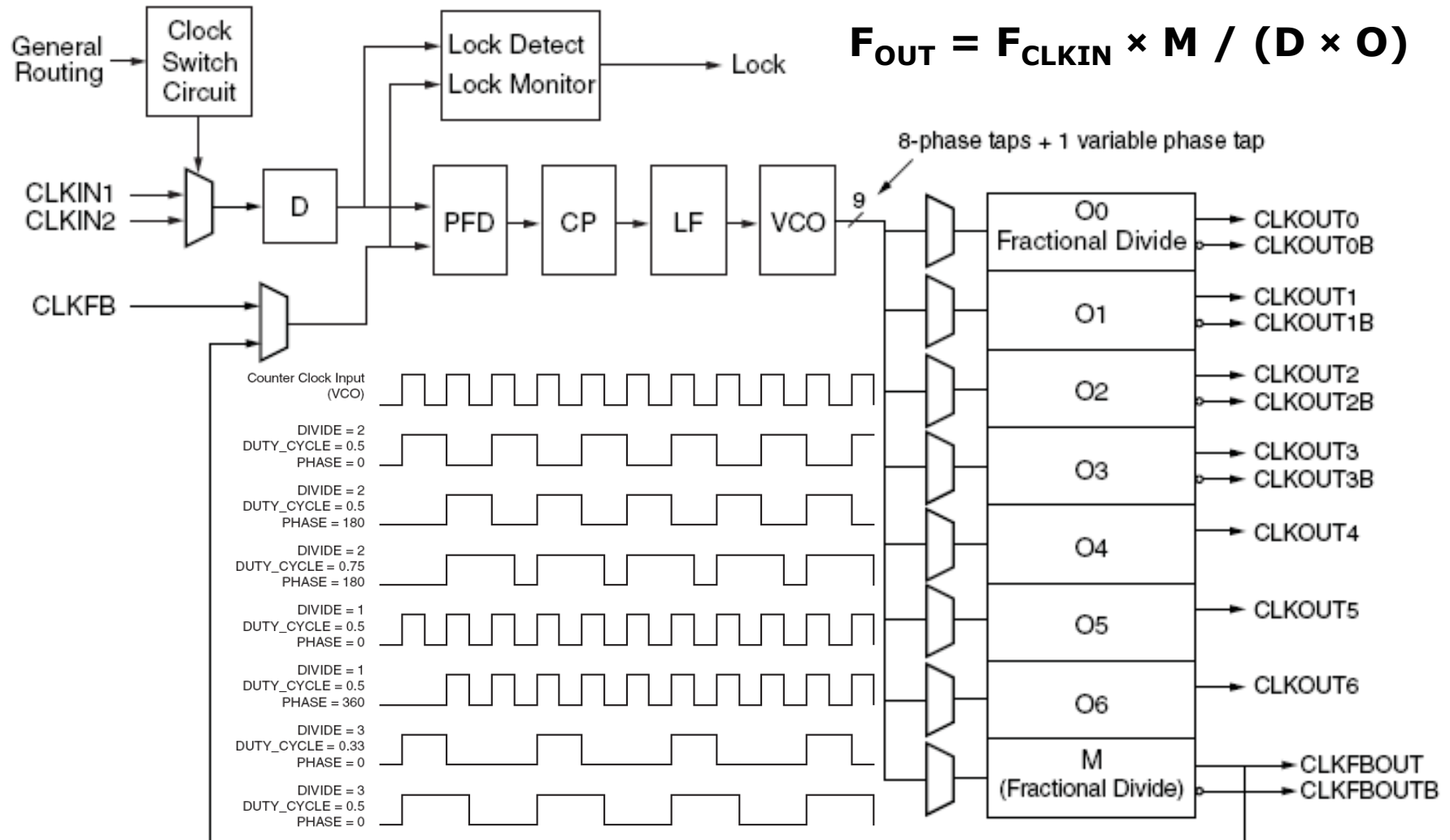
Xilinx Artix-7

Clock Management Tile

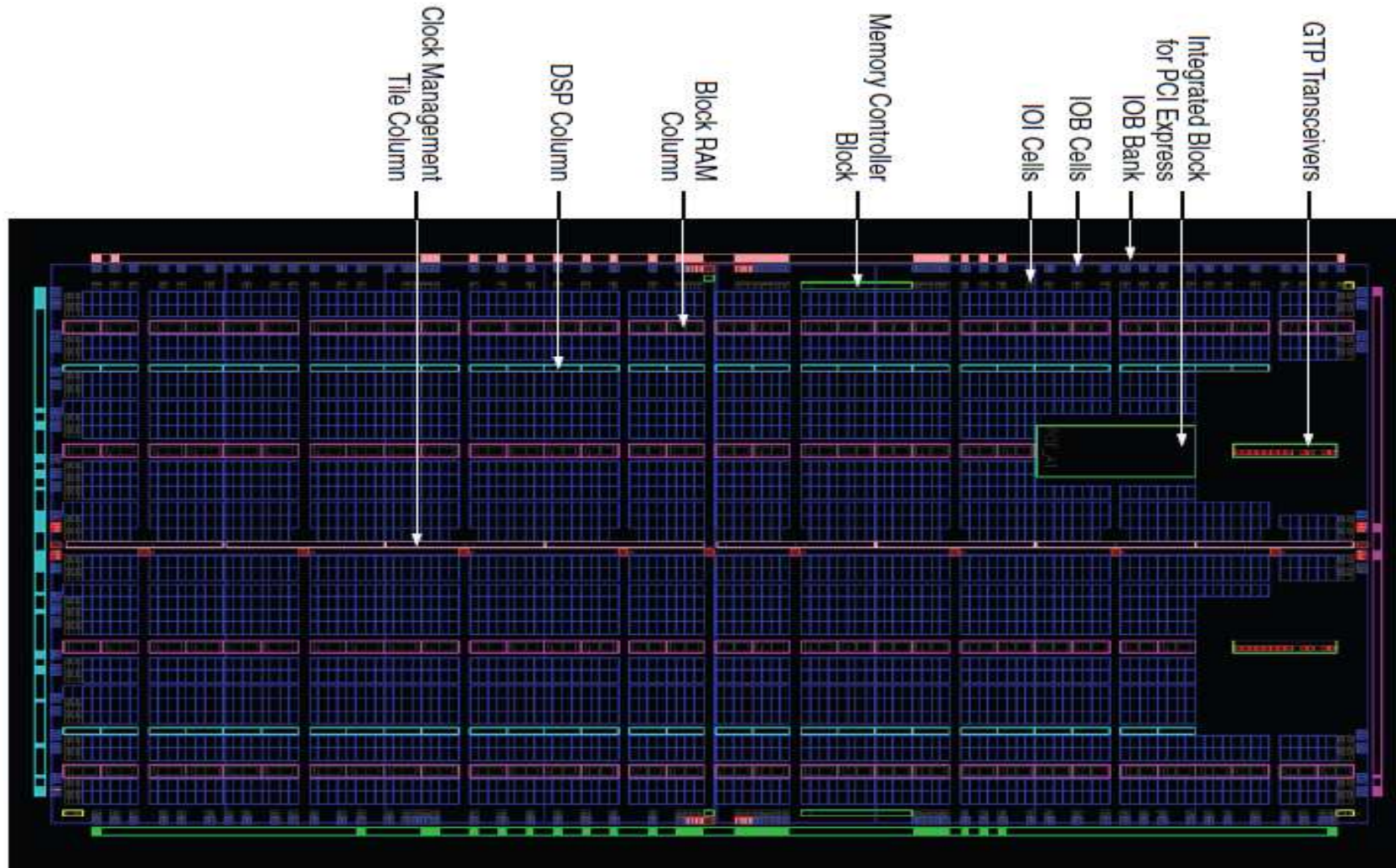
Phase Locked Loop + Mixed-Mode Clock Manager



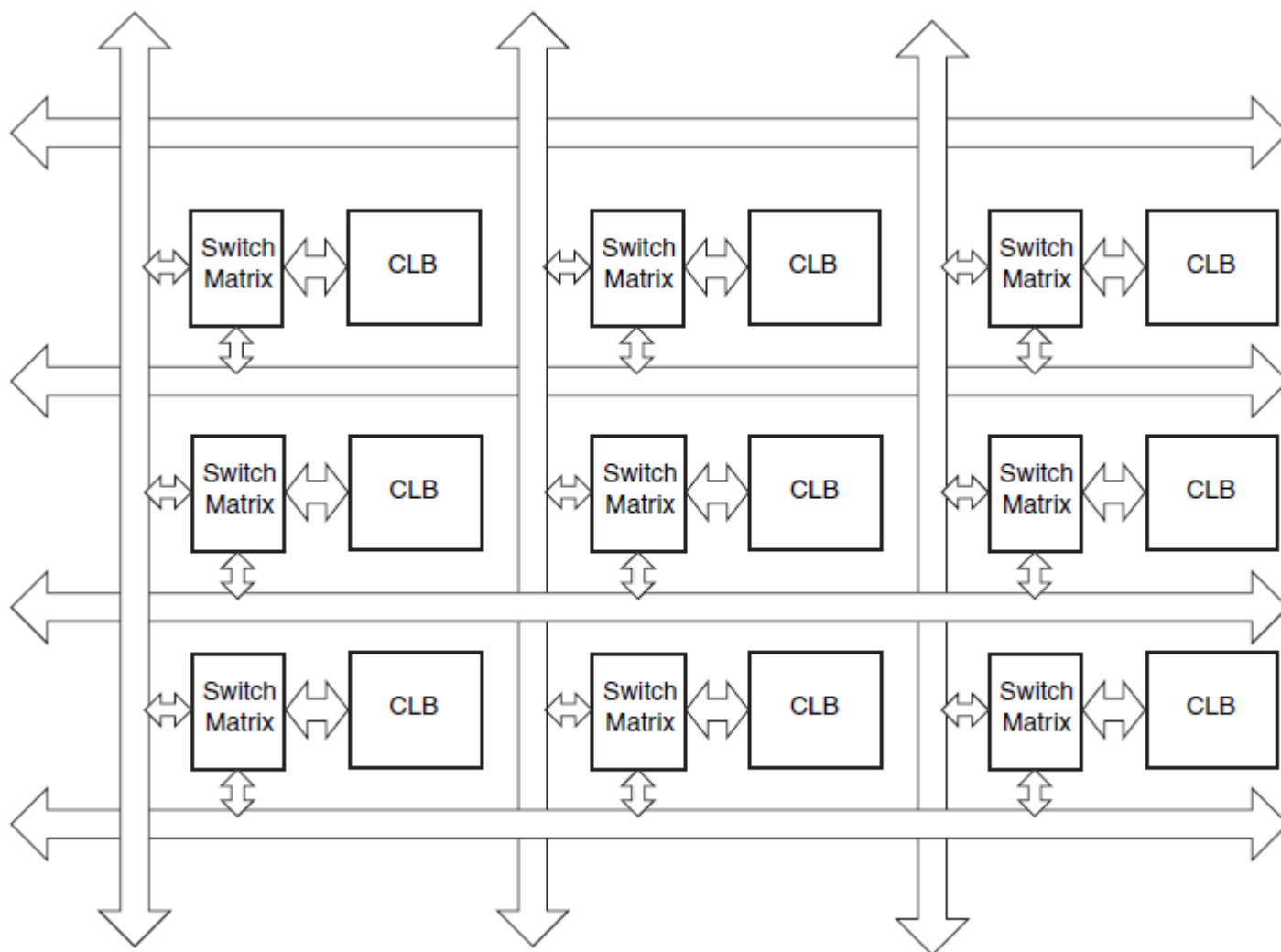
Xilinx Artix-7 Clock Management Tile Mixed-Mode Clock Manager

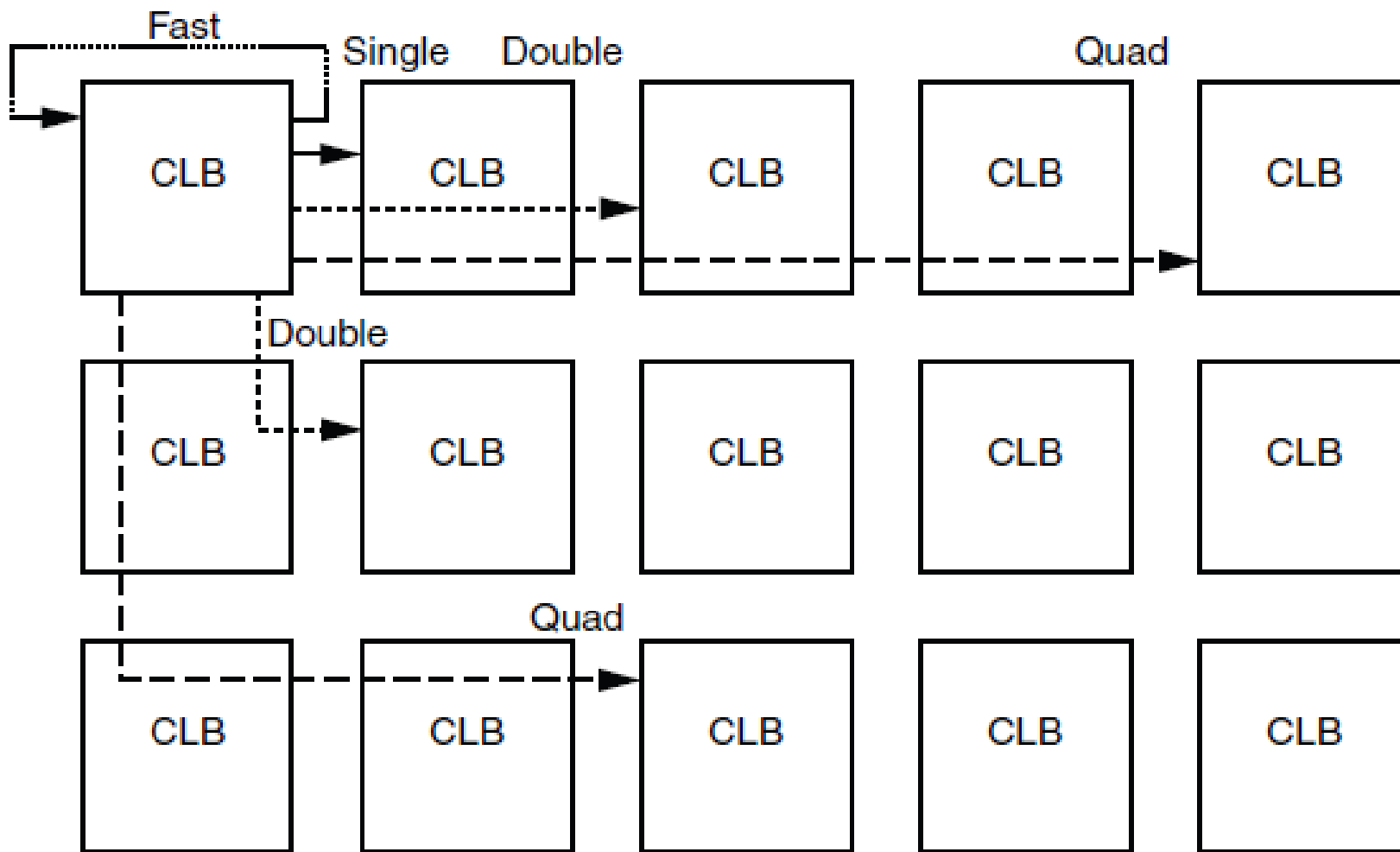


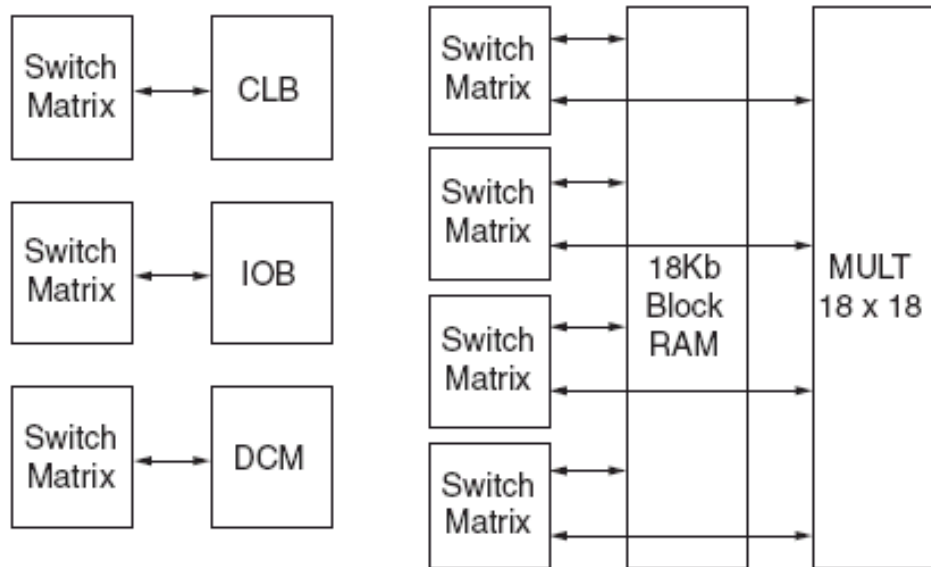
Xilinx Spartan-6 *Floorplan*



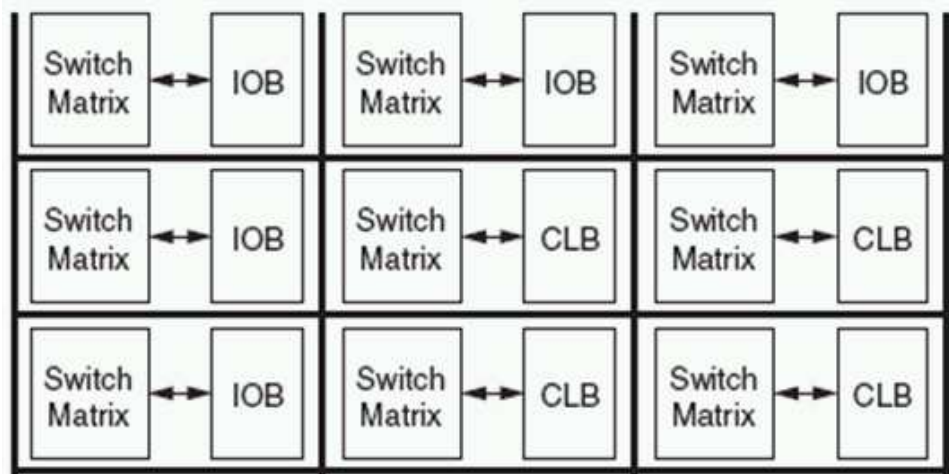
Xilinx Spartan-6 Zasoby połączeniowe





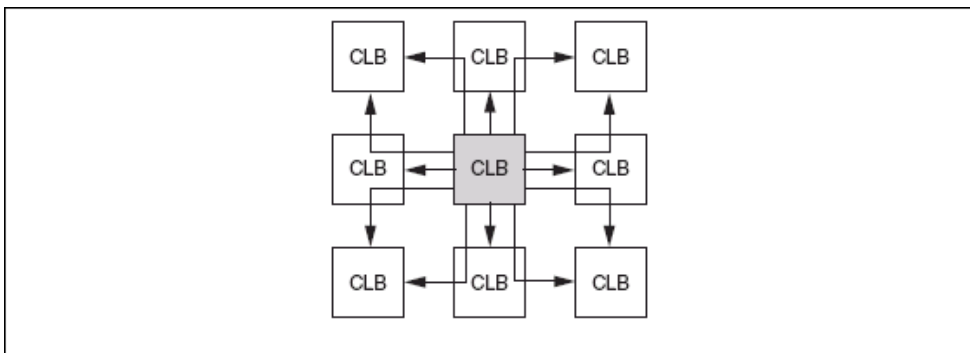
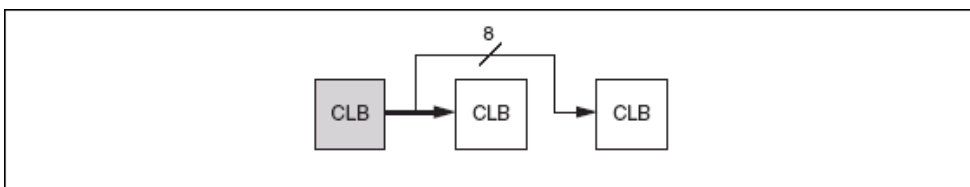
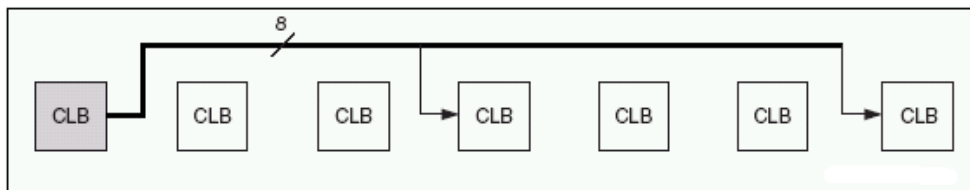
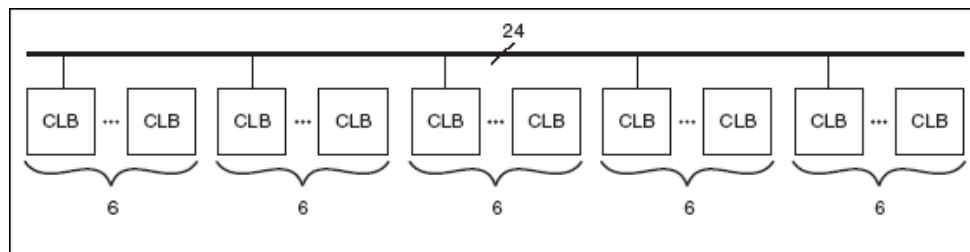


Interconnect Tile:
Switch Matrix podłączona
do elementu funkcyjnego
(CL B, IOB, DCM, BRAM, MULT)



Połączenia:

- ***long lines***
- ***hex lines***
- ***double lines***
- ***direct lines***



- 24 linie pionowe i poziome na każdy wiersz i kolumnę,
- rozciągnięte przez cały układ
- połączone co 6 Switch Matrix

- 8 linii *hex* w 4 kierunkach
- sterowanie tylko na początku
- odbiór w połowie i na końcu
- połączone co 3 Switch Matrix

- 8 linii *double* w 4 kierunkach
- sterowanie tylko na początku
- odbiór w połowie i na końcu

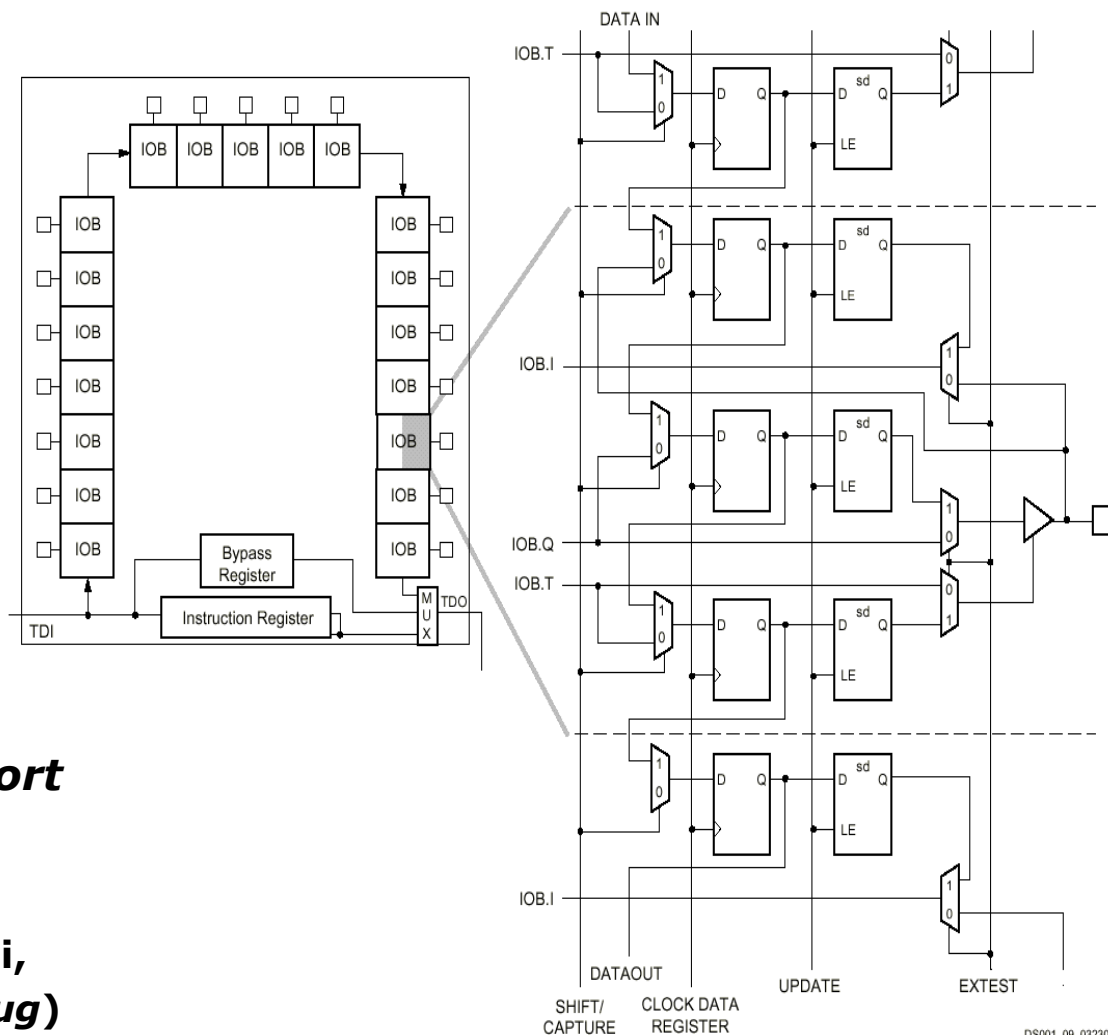
- linie *direct* w 8 kierunkach
- przekazują sygnały z/do w/w zasobów

Tryby konfiguracji:

- **Slave/Master Serial**
- **Slave/Master Parallel (SelectMAP) 8/16/32b**
- **Master SPI x1/2/4b (Serial Flash, indirect)**
- **Master BPI D16/A29 (Parallel Flash, indirect)**
- **JTAG**

Dodatkowe mechanizmy:

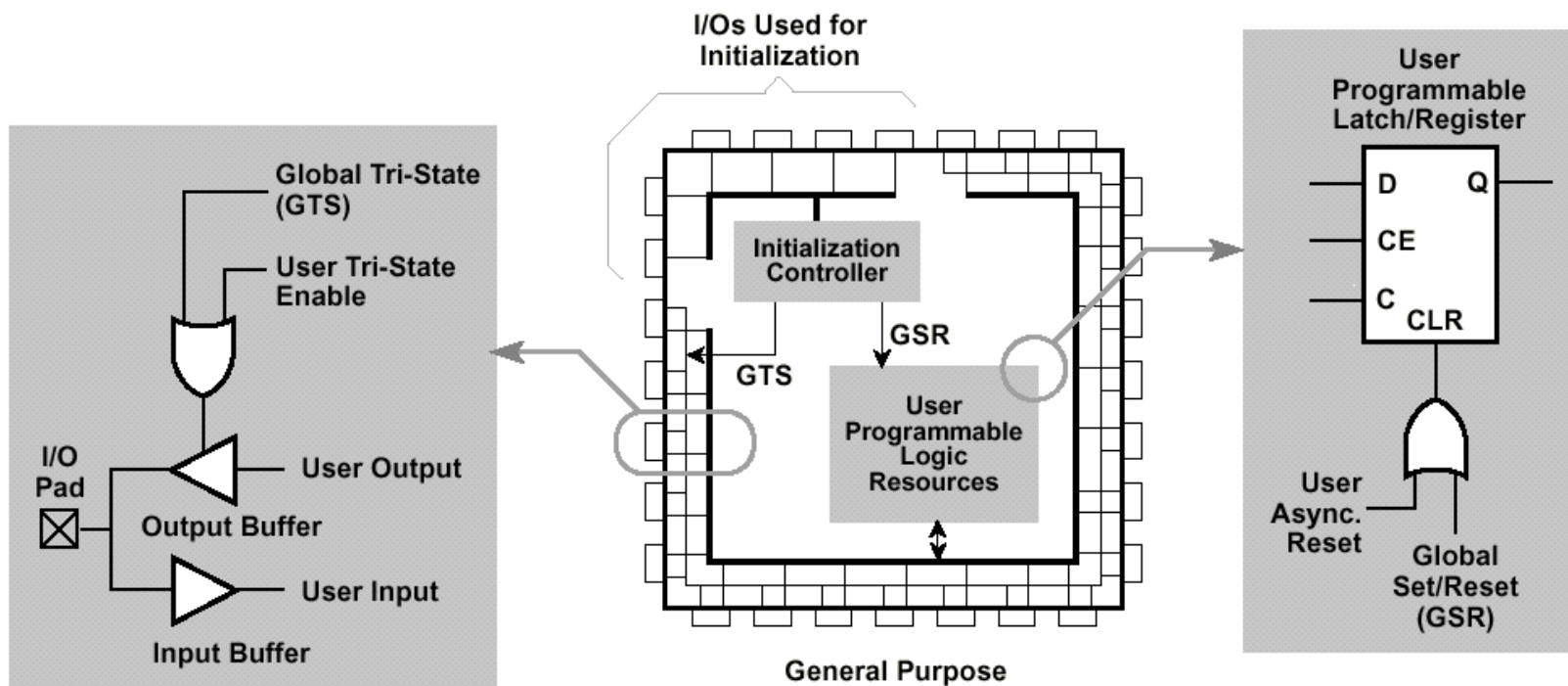
- **Multiboot / Fallback**
- **Dynamic Reconfiguration Port**
- **Bitstream encryption**
- **Readback Verify/Capture**
weryfikacja pamięci konfiguracji,
odczyt stanów elementów (*debug*)



Xilinx Artix-7

Sygnaly globalne: GSR i GTS

- **GSR** – *Global Set/Reset*
- **GTS** – *Global Tri-State*

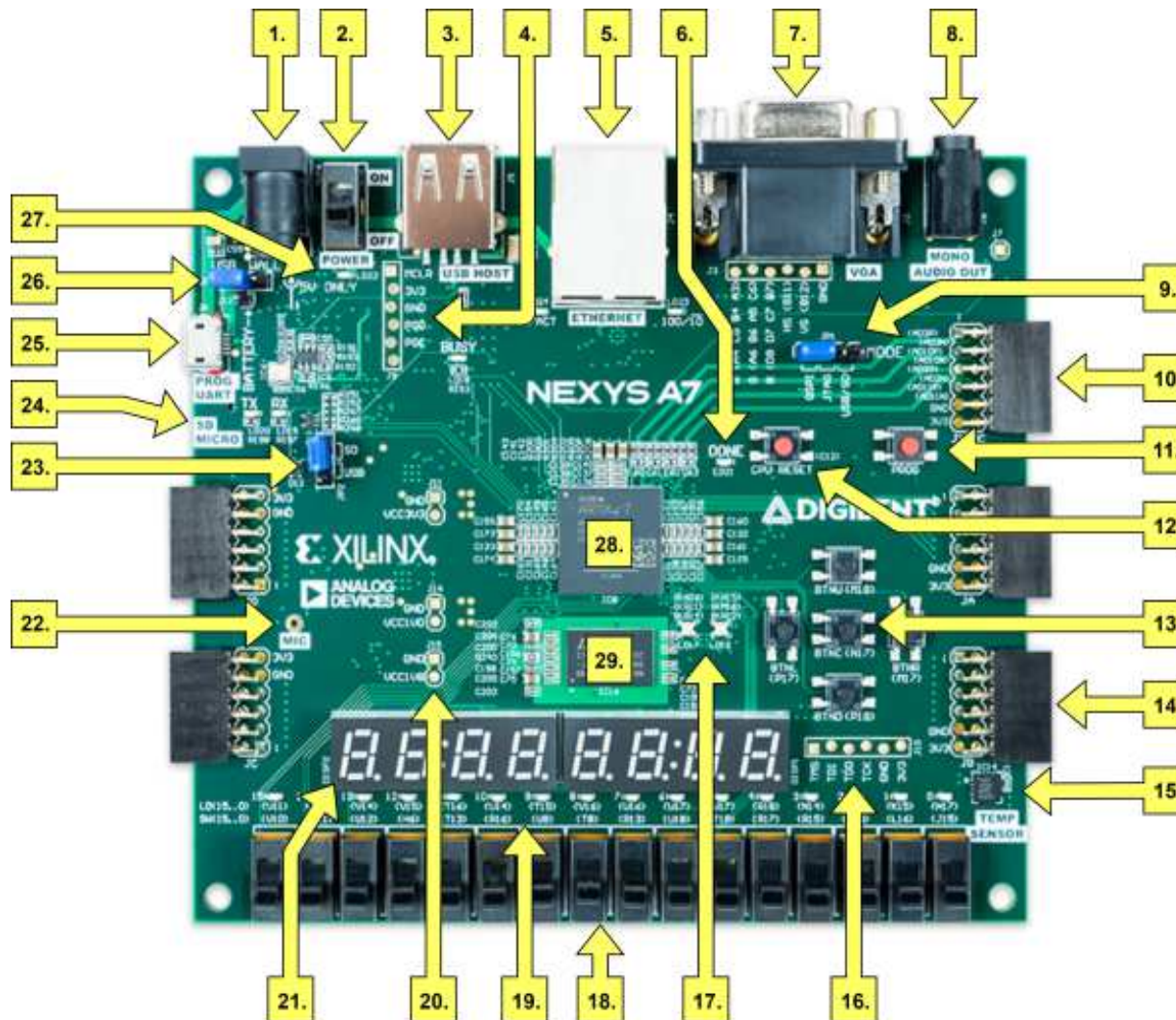


X8352

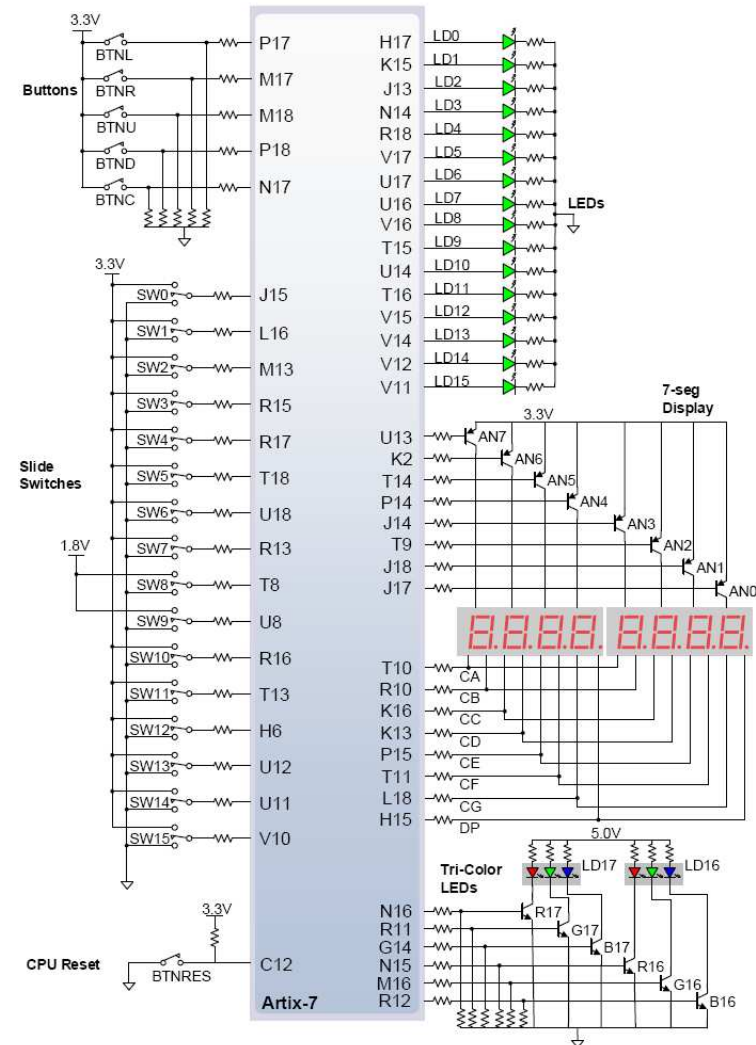
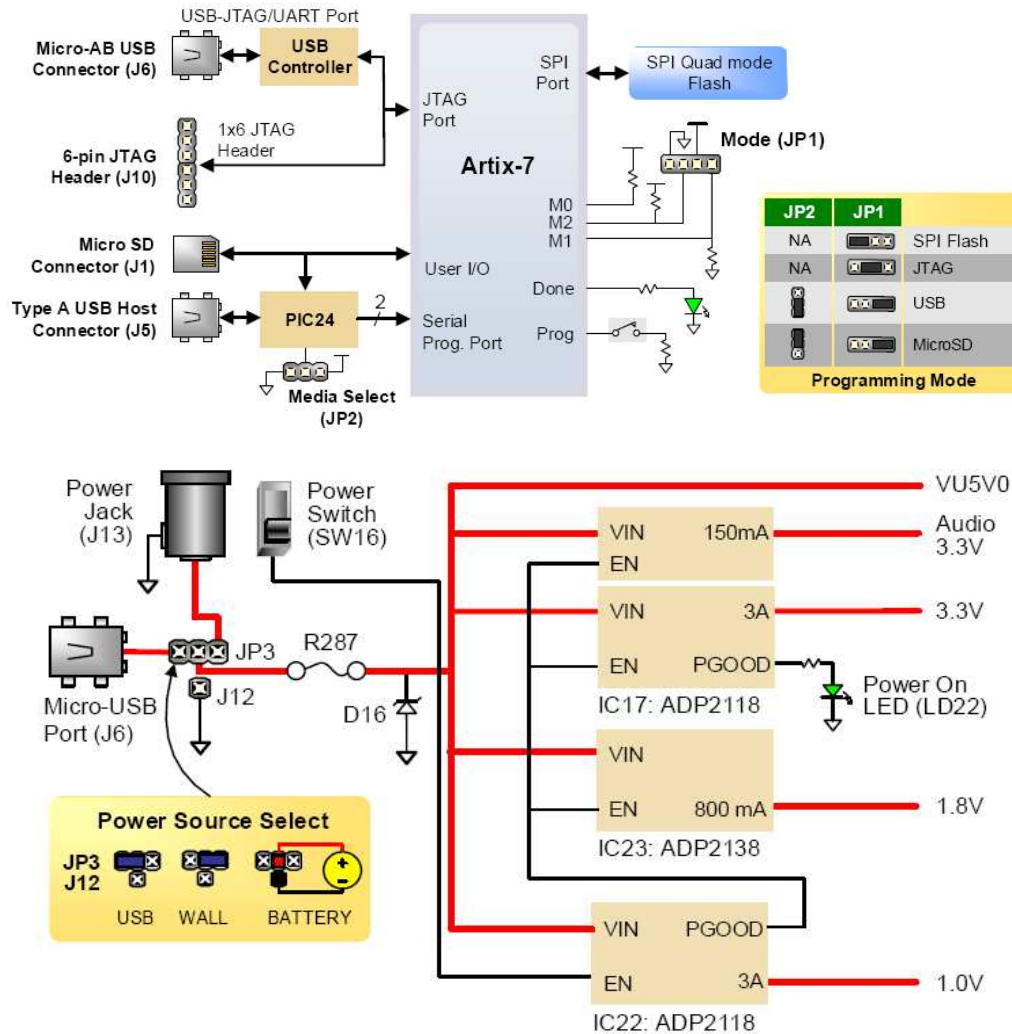


Układ XC7A100T-1CSG324C:

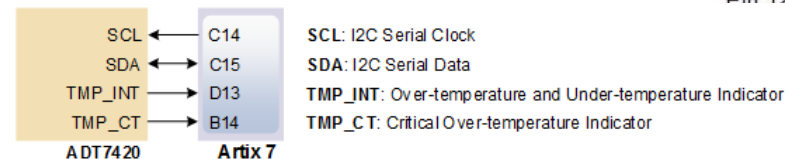
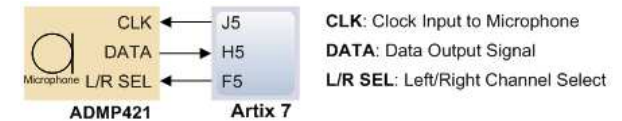
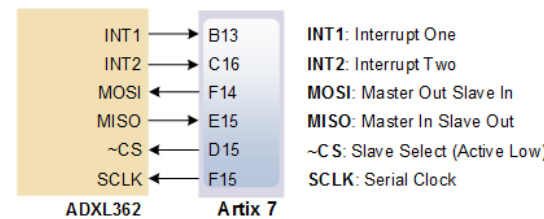
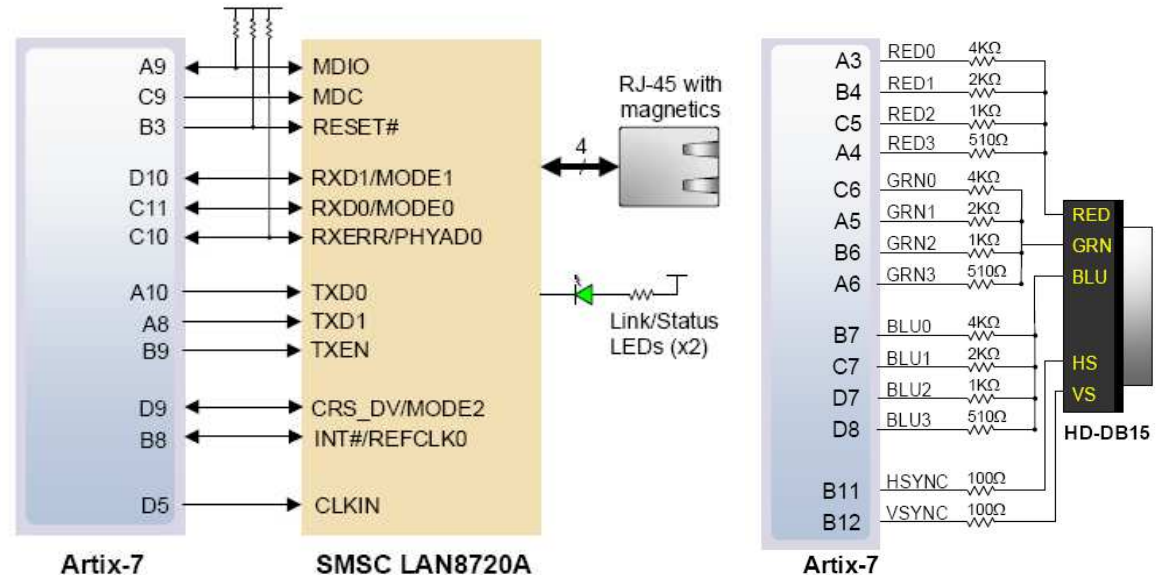
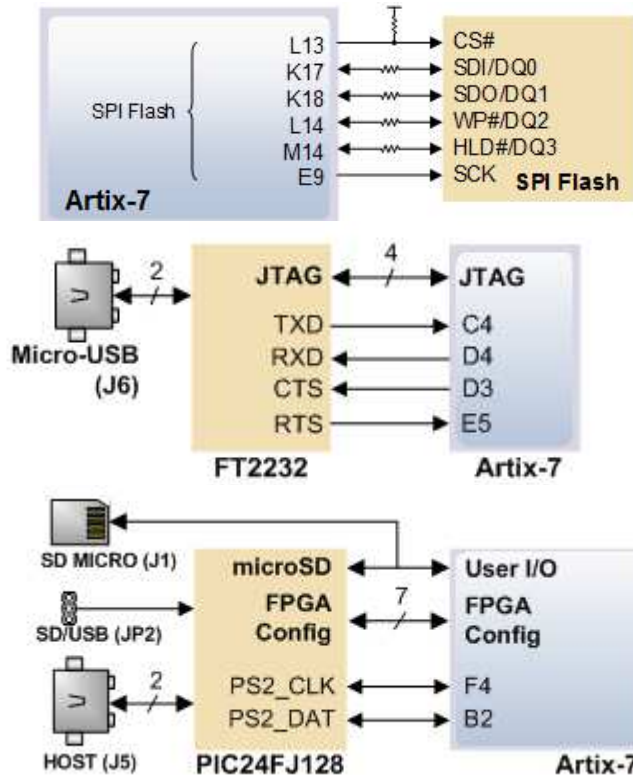
- **15,850 Logic Slices:**
 - 64,400 LUTs
 - 101,440 Logic Cells
 - 128,800 przerzutników
- **1,188Kb pamięci rozproszonej**
- **4,860Kb pamięci blokowej w 135 blokach**
- **240 bloków DSP48E1**
- **6 bloków CMT**
- **210 user I/Os w 6 bankach**



- 1 Power jack
- 2 Power switch
- 3 USB host connector
- 4 PIC24 programming port (factory use)
- 5 Ethernet connector
- 6 FPGA programming done LED
- 7 VGA connector
- 8 Audio connector
- 9 Programming mode jumper
- 10 Analog signal Pmod port (XADC)
- 11 FPGA configuration reset button
- 12 CPU reset button (for soft cores)
- 13 Five pushbuttons
- 14 Pmod port(s)
- 15 Temperature sensor
- 16 JTAG port for (optional) external cable
- 17 Tri-color (RGB) LEDs
- 18 Slide switches (16)
- 19 LEDs (16)
- 20 Power supply test point(s)
- 21 Eight digit 7-seg display
- 22 Microphone
- 23 External configuration jumper (SD/USB)
- 24 MicroSD card slot
- 25 Shared UART/ JTAG USB port
- 26 Power select jumper and battery header
- 27 Power-good LED
- 28 Xilinx Artix-7 FPGA
- 29 DDR2 memory



Setting	Value
Memory type	DDR2 SDRAM
Max. clock period	3000ps (667Mbps data rate)
Recommended clock period (for easy clock generation)	3077ps (650Mbps data rate)
Memory part	MT47H64M16HR-25E
Data width	16
Data mask	Enabled
Chip Select pin	Enabled
Rtt (nominal) – On-die termination	50ohms
Internal Vref	Enabled
Internal termination impedance	50ohms



Ciąg dalszy
nastąpi...

